# Curriculum Vitae

***Mrs. Patel Vibhaben Divyeshbhai***
***vibhadp@iitk.ac.in***

## *Personal Details*

**Permanent Address**: 9/A, Janpad Society,
Opposite Scoutt Bhavan,
P. T. College Road, Paldi
Ahmedabad - 380 007.

**Temporary Address:** C-314, Girls Hostel - I , IIT-Kanpur
Kanpur – 208016, Uttarpradesh.

**Phone No**: (M) 9005751922 (R) (079) 26672450

## *Academic Oualification*

| Sr. No. | Examination/Degree | Board/ University | Month & Year | CPI / % | Class | Main Subject |
|---|---|---|---|---|---|---|
| 1 | Ph.D. | IIT Kanpur | In progress | 8.5 CPI | - | Computer |
| 2 | M. E. Computer | S. P. Uni. | Sep.-2004 | 71.44 % | Distinction | Computer |
| 3 | B.E. Computer | Gujarat Uni. | July-1998 | 66 % | Distinction | Computer |
| 4 | 12th | HSEB | Mar.-1994 | 81 % | Distinction | Maths/Sci. |
| 5 | 10th | GSEB | Mar.-1992 | 79 % | Distinction | Science |

**Area of Ph.D. Research**
HPC using Graphics Processing Unit

## *Experience*

| Academics | Research | Industry | Others | Total |
|---|---|---|---|---|
| 9 years | 1 year | - | - | 10 year |

**Specific Details of Experience: (In Chronological Order)**

| Sr. No. | Organization | Period (From To) (dd-mm-yyyy) | Designation |
|---|---|---|---|
| 1. | Nirma University of Sci. and Technology | 24/05/2008 to till date | Associate Professor |
| 2. | Nirma University of Sci. and Technology | 24/05/2005 to 23/04/05 | Assistant Professor |
| 3. | Nirma Institute of Technology | 01/02/01 to 23/5/2005 | Lecturer |
| 5. | Shri Chimanbhai Patel Institute of Computer Applications | 09/08/99 to 31/01/2001 | Lecturer |

## *Projects at Undergraduate Level*

1. Weighing Scale Interfacing Software for Uttam Dairy in 6th Semester
2. Grapher in ‘C’ as final semester project at PRL

## *Skills*

1. **Programming Languages :** C, C++, Java, 8085 & 8086 Assembly language,
2. **Operating Systems :** Microsoft Windows, Linux.
3. **Tools :** Matlab, Lex, Yacc, LaTEX, Rational requisite Pro

## *Subject taught at Undergraduate Level*

1. Programming Language – I
2. System Programming
3. Data Structures and Algorithms
4. Computer Architecture and Peripherals
5. Advanced Computer Architecture
6. Advanced Database Management System
7. Parallel Computing
8. Microprocessor Architecture and Interfacing
9. Advanced Microprocessor

## *Seminar/ Workshop / Conference attended:*

1. Attended a National Conference on Computer vision, Pattern Recognition, Image processing and graphics. at DAIICT, January 11-13, 2008.
2. Attended a Summer Course on Program Optimization for Multicore Architectures, at IIT Kanpur , July 2-7, 2007.
3. Attended five days technology workshop on " Optimizing Performance of Parallel Programs on Emerging Multi-Core Processors & GPUs (OPECG-2009)" at IIT Madras, June 1-5, 2009.
4. Attended workshop on "Architectures and Compilers for Multithreading" at IIT Kanpur, December 13-15, 2007.

## *Academic Administrative Experience*

- Worked as Section Head of Information Technology department for two years.
- Worked as Joint Examination Coordinator for two years at Institute of Technology, Nirma University.
- Member of Core Committee of Cultural Programme
- Examination coordinator for Mid Semester Examination and Semester End Examination
- Responsible for maintenance of B-201 Laboratory for one year

## *Seminars/Expert Talks conducted*

1. One day Seminar on "Internals of TCP/IP" on 3rd October 2004. at AES Institute of Computer Studies in association with Computer Society of India.

## *Research Experience*

| | | |
|---|---|---|
| **1** | **Ph.D** | High Performance Computing using Graphics Processing Unit |
| | Guide Name | Prof. Sanjeev Kumar Aggarwal |
| | Organization | IIT-Kanpur |
| | Description | Multicore and Many core architectures have emerged as an elegant solution to meet the increased computational requirements of current applications while avoiding problems like chip overheating. However, adopting these architectures has been a process plagued with legacy issues. The problem of partitioning existing single-threaded applications so as to maximally utilize the multiple cores has been a challenging one. CUDA is a one of several programming models which provides high performance implementations for general purpose computational tasks. However, manual development of optimized CUDA code for efficient data access is a difficult task. Hence, source to source translation of sequential programs to efficient multi-threaded CUDA programs is of interest for GPGPU programmers. |
| **2** | **M.Tech thesis** | Comparison of PCA and Subspace LDA for face Recognition |
| | Guide Name | Prof. Darsak Thakore |
| | Organization | ISTAR |
| | Description | Implemented two linear dimensionality reduction techniques which include Principal Component Analysis and Subspace Linear Discriminant Analysis on ORL Database and compared their results over various thresholds using Euclidean Distance. |

**Other Details:-**

- **TRAINING INFORMATION :**
  **Training Center During BE :** PRL (Physical Research Laboratory).(A'bad)
- **MEMBER OF PROFESSIONAL BODIES**
  1. Life member OF COMPUTER SOCIETY OF INDIA.
  2. Life member of ISTE

Declaration: The above information is correct to the best of my knowledge.
Vibha Patel