CS748 - ARITHMETIC CIRCUIT COMPLEXITY

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MID-SEMESTER EXAMINATION (2018-19/II)

POINTS: 50

DATE GIVEN: 13-FEB DUE: 19-FEB-2019 (6PM)

Rules:

- You are not allowed to discuss.
- Write the solutions on your own and honorably *acknowledge* the sources if any. `http://cse.iitk.ac.in/pages/AntiCheatingPolicy.html`
- Clearly express the fundamental *idea* of your proof/ algorithm before going into the other proof details. The distribution of partial marks is according to the proof steps.
- There will be a penalty if you write unnecessary or unrelated details in your solution. Also, do not repeat the proof details covered before.

Question 1: *[15+5 points]* Let us introduce a *division* gate in the arithmetic circuit model. Let $f \in \mathbb{C}[x_1, \ldots, x_n]$ be a degree d polynomial computed by a circuit of size s, using $\{+, \times, \div\}$ gates. Show that f has a circuit of size poly(sd) using only the $\{+, \times\}$ gates.

Generalize the above result to any characteristic.

The depth reduction proofs unfold several structural properties of arithmetic circuits. Two of them will be discussed below.

Question 2: *[15 points]* VNP was defined by taking projections of a circuit $C(\mathbf{x}, \mathbf{y})$, in $\mathbf{y} \in \{0,1\}^n$. Analogously, define VNP$_e$ by taking the sum of all projections of a *formula* $F(\mathbf{x}, \mathbf{y})$, in $\mathbf{y} \in \{0,1\}^n$.

Show that VNP = VNP$_e$.

Question 3: *[5+10 points]* A circuit C is called *weakly-skew* if each of its multiplication gate α has two inputs β and γ such that: at least one of the subcircuits C_β or C_γ is connected to the rest of the circuit only via α.

The class of VP-polynomials computed by a poly-sized weakly-skew circuit is called VP$_{ws}$.

Show that *det is VP_{ws}-complete*, i.e. det is in this class and that any polynomial in the class is a projection of det.

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