## Parity not in AC<sup>0</sup>

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## Definition 1: (Boolean circuits)[ASB]

For every  $n \in N$ , an *n*-input single output Boolean circuit is a directed acyclic graph with *n* sources (vertices with no incoming edges) and one sink (vertex with no outgoing edges). All non-source vertices are called gates and are labeled with one of OR, AND, and NOT. The size of *C*, denoted by |C|, is the number of vertices in it.

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If *C* is a Boolean circuit, and  $x \in \{0, 1\}$  is some input, then the output of *C* on *x*, denoted by C(x), is defined in the natural way. More formally, for every vertex *v* of *C* we give it a value val(v) as follows: if *v* is the *i*<sup>th</sup> input vertex then  $val(v) = x_i$  and otherwise val(v) is defined recursively by applying *v*'s logical operation on the values of the vertices connected to *v*. The output C(x) is the value of the output vertex.

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## Definition 2: (Circuit families and language recognition)[ASB]

Let  $T : N \to N$  be a function. A T(n)-size circuit family is a sequence  $\{C_n\}$   $n \in N$  of Boolean circuits, where  $C_n$  has n inputs and a single output, and its size  $|C_n| \leq T(n)$  for every n.

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We say that a language L is in SIZE(T(n)) if there exists a T(n)-size circuit family { $C_n$  }  $n \in N$  such that for every  $x \in \{0, 1\}^n$ ,  $x \in L \Leftrightarrow C_n(x) = 1$ .

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## Definition 4: (k-CNF)

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### Definition 5: (*k*-DNF)

A boolean formula that is an OR of AND's where each AND involves at most k variables.

#### Definition 6: (Random Restriction)

Let f is a function on n variables. A random restriction  $\rho$  is a partial assignment that assigns random values to t < n randomly selected variables of f. We denote the random restriction of f under  $\rho$  by  $f|_{\rho}$ . That is,  $f|_{\rho}$  takes an assignment  $\tau$  to the variables not assigned by  $\rho$  as input, and outputs f applied to  $\rho$  and  $\tau$ .

## Theorem 1([FSS81, Ajt83])

Let **PARITY** = { $x \in \{0, 1\}^n$  : x has odd number of 1's}. Then **PARITY**  $\notin AC^0$ .

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## Proof Sketch [ASB]

The main tool in the proof of Theorem 1 is the concept of random restrictions. Let f be a function computable by a depth d circuit of polynomial size and suppose that we choose at random a vast majority (i.e.,  $n n^{\epsilon}$  for some constant  $\epsilon > 0$  depending on d) of the input variables and fix each such variable to be either 0 or 1 at random. By Hastad's switching lemma, it is clear that with positive probability, the function f subject to this restriction is constant (i.e., it is either always zero or always one). Since the parity function cannot be made a constant by fixing values to a subset of the variables, it follows that it cannot be computed by a constant depth polynomial-sized circuit.

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Moreover the simplified circuit has size poly(S) and depth O(d).

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- We do this untill the depth of circuit becomes 2.

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- Suppose that bottom level of circuit contains AND gates. Therefore the level above it contains OR gates.
- Observe that each OR gate computes a k<sub>i</sub>-DNF.
- Apply switching lemma to the function computed by this gate.

If f is a function that is expressible as a k-DNF and  $\rho$  is a random restriction that assigns random values to t randomly selected input bits, then  $\forall s \geq 2$ 

$$\Pr_{\rho}[f|_{\rho} \text{ is not expressible as } s\text{-}CNF] \leq \left(\frac{(n-t)k^{10}}{n}\right)^{s/2} \tag{1}$$

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Note that by applying this lemma to  $\neg f$  we get the same result with the terms DNF and CNF interchanged.

• By switching lemma, with probability 1 -  $\left(\frac{k_i^{10}}{n^{\frac{1}{2^{i+1}}}}\right)^{\frac{k_{i+1}}{2}}$ , we can convert this  $k_i$ -DNF to  $k_{i+1}$ -CNF.

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- Note that we are free to choose any  $k_i \ge 2$ .
- So we choose  $k_i = 10b2^i$ .

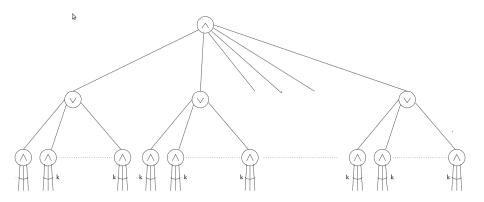


Figure: Circuit before Hastad switching transformation.[ASB]

PARITY ∉ AC<sup>0</sup>

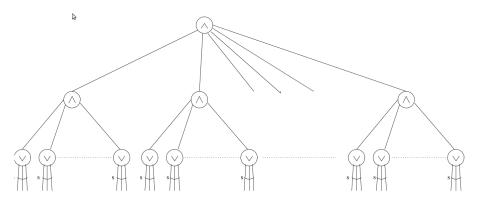


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- So we choose  $k_i = 10b2^i$ .
- Since the top level gate of  $k_{i+1}$ -CNF is AND, and since gates can have unbounded fan-in, we can merge this AND gate with the AND gate above it reducing the depth of the circuit by 1.

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- We can make such a formula constant by fixing atmost k variables.
- But the parity function can not be made constant under any restriction of less than *n* inputs.
- We get a contradiction. Therefore our assumption is wrong. Hence **PARITY**  $\notin AC^0$ .



[FSS81] M. Furst, J. Saxe, and M. Sipser (1981),Parity, circuits, and the polynomial time hierarchy,Mathematical Systems Theory 17:1327, 1984. Prelim version FOCS 81.



 $\sum 1$  -formulae on finite structures,

Annals of Pure and Applied Logic 24:148.



[ASB] Arora, Sanjeev; Barak, Boaz (2009),

Computational Complexity: A Modern Approach, Cambridge, p. 248-249.

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