Computer Architecture

SIMD Architecture: Overview

Debadatta Mishra, CSE, IITK

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Agenda for remaining lectures

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CS423

Overview of SIMD processing

- Same operation on multiple data items. Example: ***Y*** = *a* * ***X*** + ***Y*** ***X*** and ***Y*** are vectors and *a* is a scalar. Implementation using SISD?

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SISD

```
// r1 = &x[0], r2 = &y[0], element size = 8
// size of the vectors = 64

ldD f0,(a)           //load scalar a
daddiu r3,r1, #512   //r3=&X[0] + 512
loop: ldD f1,0(r1)   // f1 = x[i]
mulD f1,f1,f0        // f1 = x[i]*a
ldD f2,0(r2)         // f2 = y[i]
addD f2,f1,f2        // f2 = y[i]+a*x[i]
sD f2,0(r2)          // y[i] = y[i]+a*x[i]
daddiu r1,r1,#8      // r1 = &x[i+1]
daddiu r2,r2,#8      // r2 = &y[i+1]
sub r4,r3,r1         // elements remaining
benz r4, loop
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- #of instructions executed?
- Branch related instructions?
- Dependencies?

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- #of instructions executed? 578
- Branch related instructions? 4 out of 9 in each iteration of the loop
- Dependencies? Multiple dependencies in each iteration

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SIMD (using vector processing)

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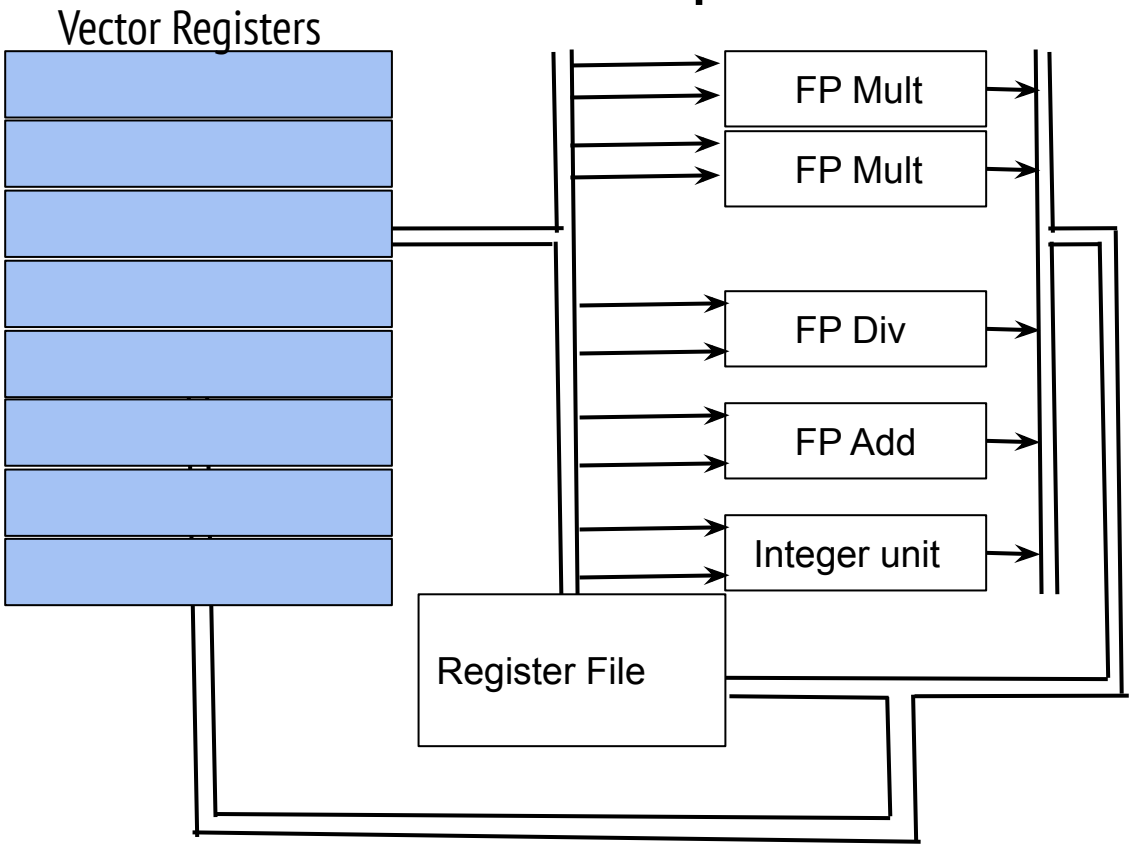
- Reduction in #of instructions
- Data forwarding through chaining (more about thing in coming slides)

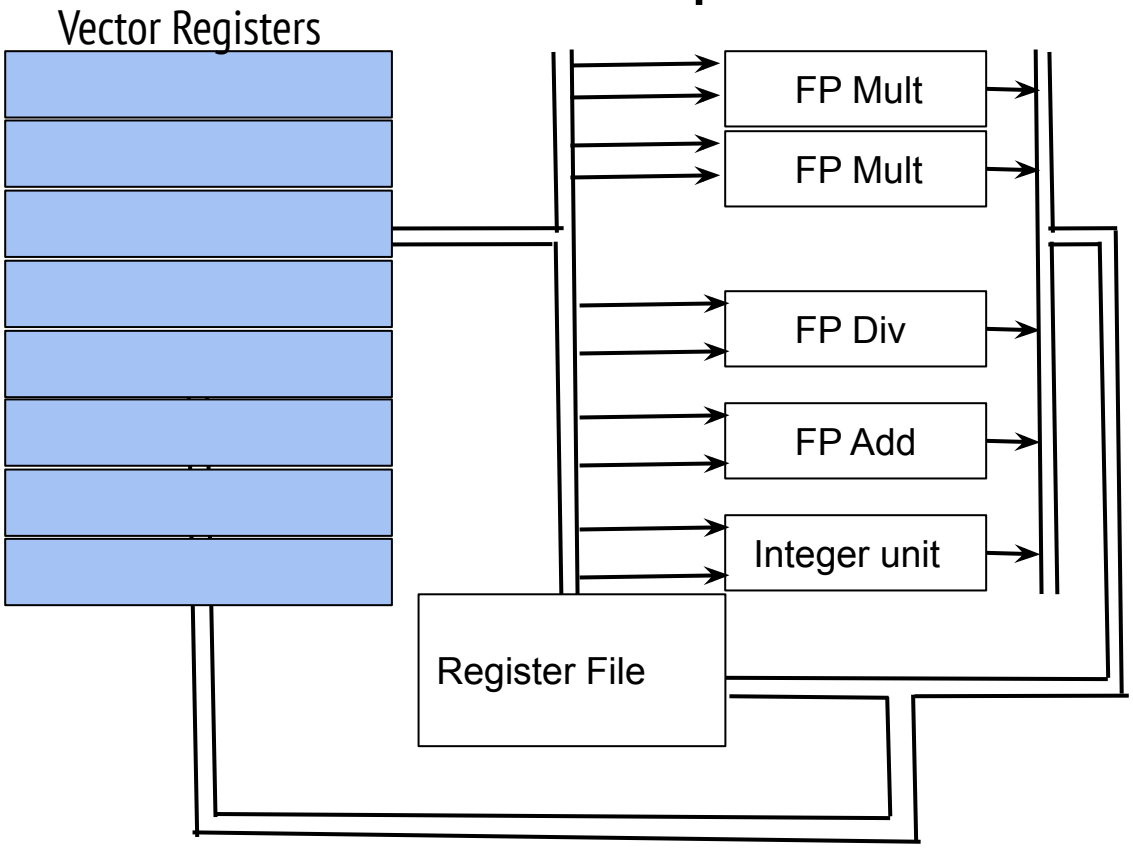
Structure of a vector processor



Vector registers

- Each register holds a single vector of length N
- Each element of the vector can be a 64-bit value
- Considering 8 vector registers of length 64, how many read/write ports are required?

Structure of a vector processor



Special vector registers

- Why special vector registers are needed?

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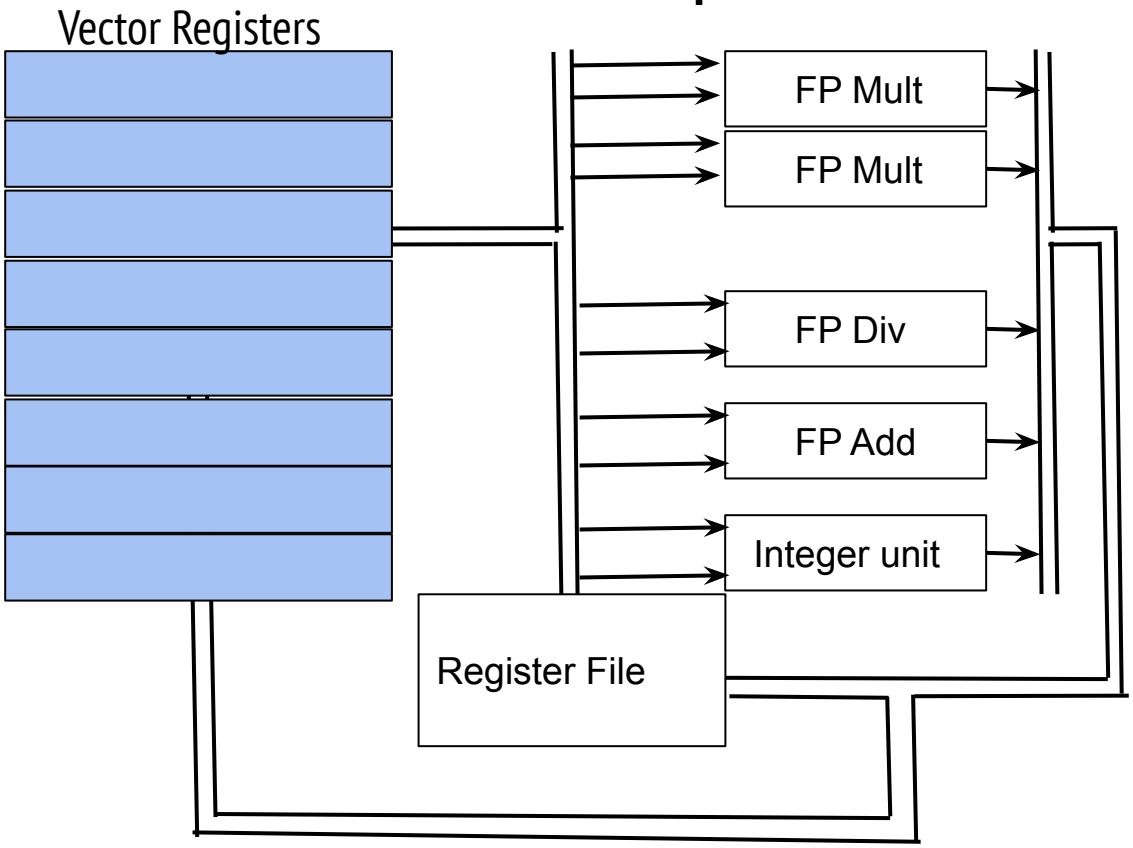
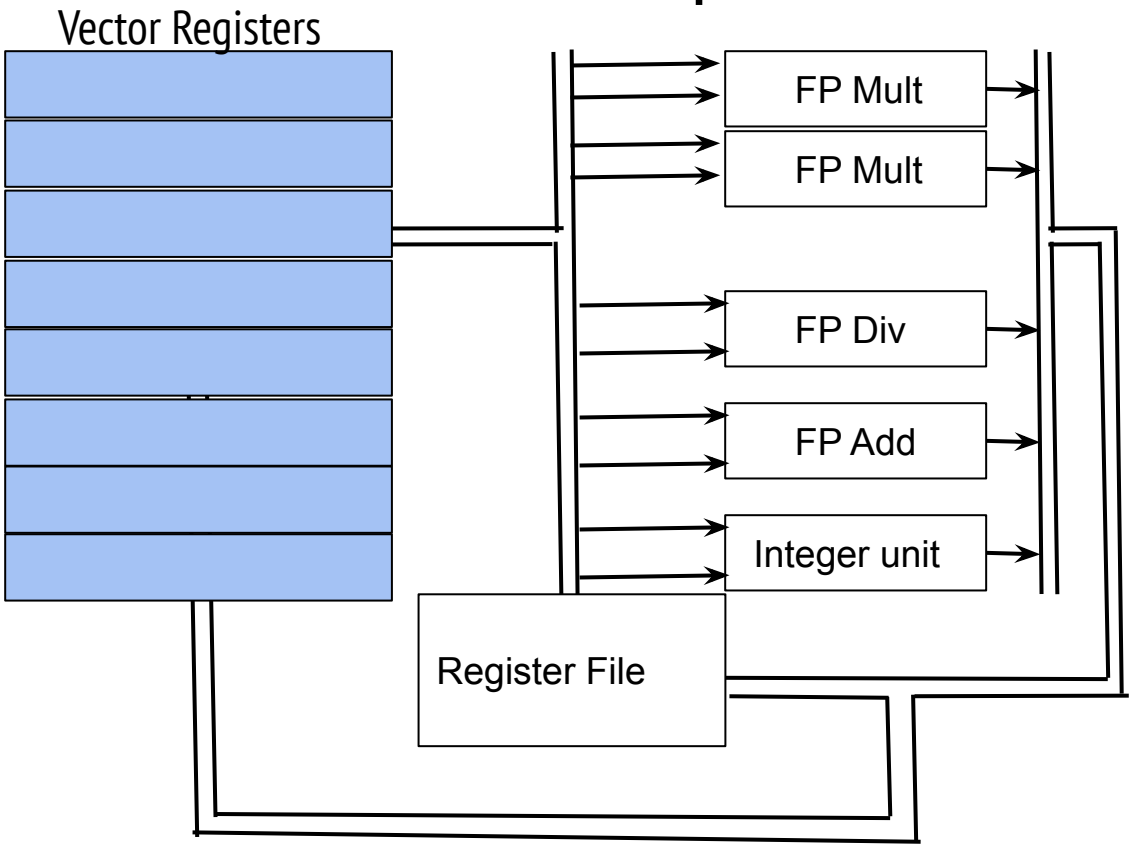


Special vector registers

- Why special vector registers are needed?
- VLEN: Vector length register to handle variable length vector operations
- VMASK: Mask register to support conditional execution. Typically a boolean vector of size N

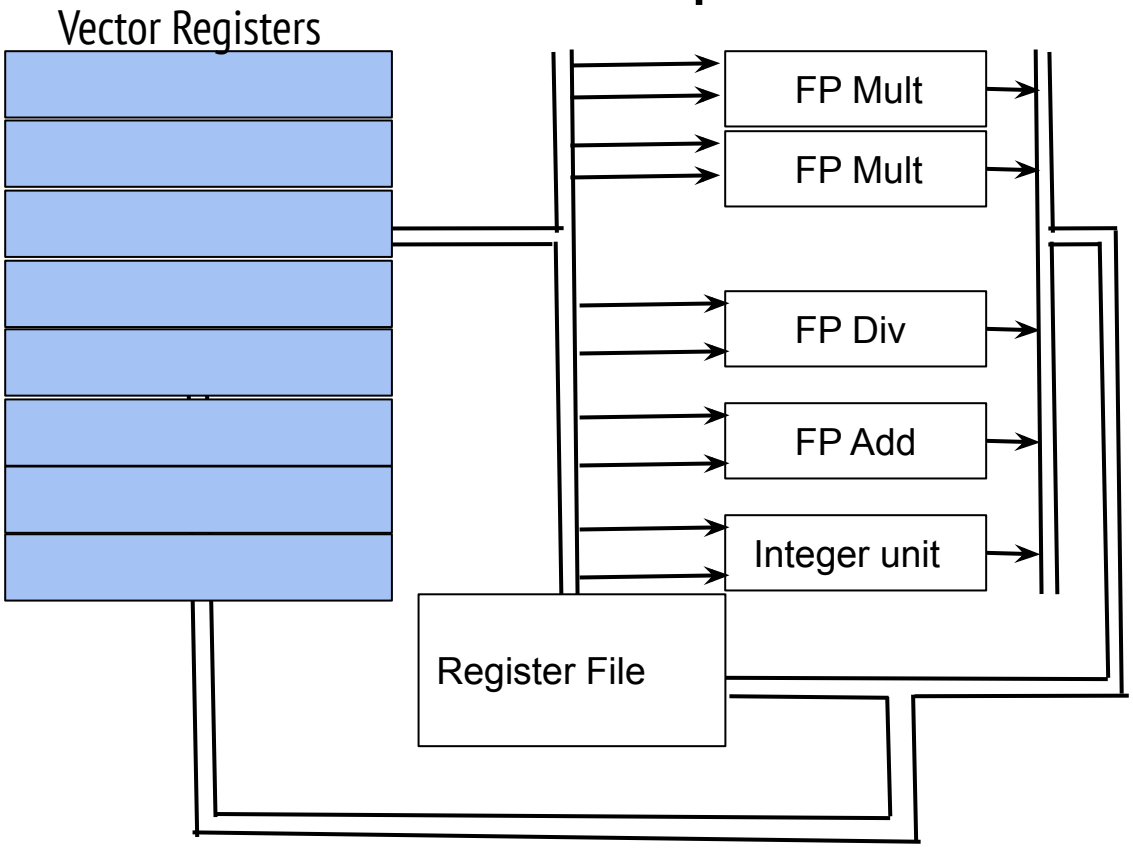
Structure of a vector processor



Vector functional units

- Each FU is pipelined with control units (for hazard detection)
- After initial fill, the can complete one operation every cycle
- Can be single lane or multiple lanes of pipeline

Structure of a vector processor



Vector load/store unit

- Pipelined load/store unit
- After the initial latency, one element can be moved between VR and memory in every cycle

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- How a single vector instruction is executed?
- Assuming a 5-stage multiplier, how many cycles to execute “mulVS” instruction for a vector of size 64?

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- Instructions not causing any structural hazard can be grouped to convoys
- How many convoys?

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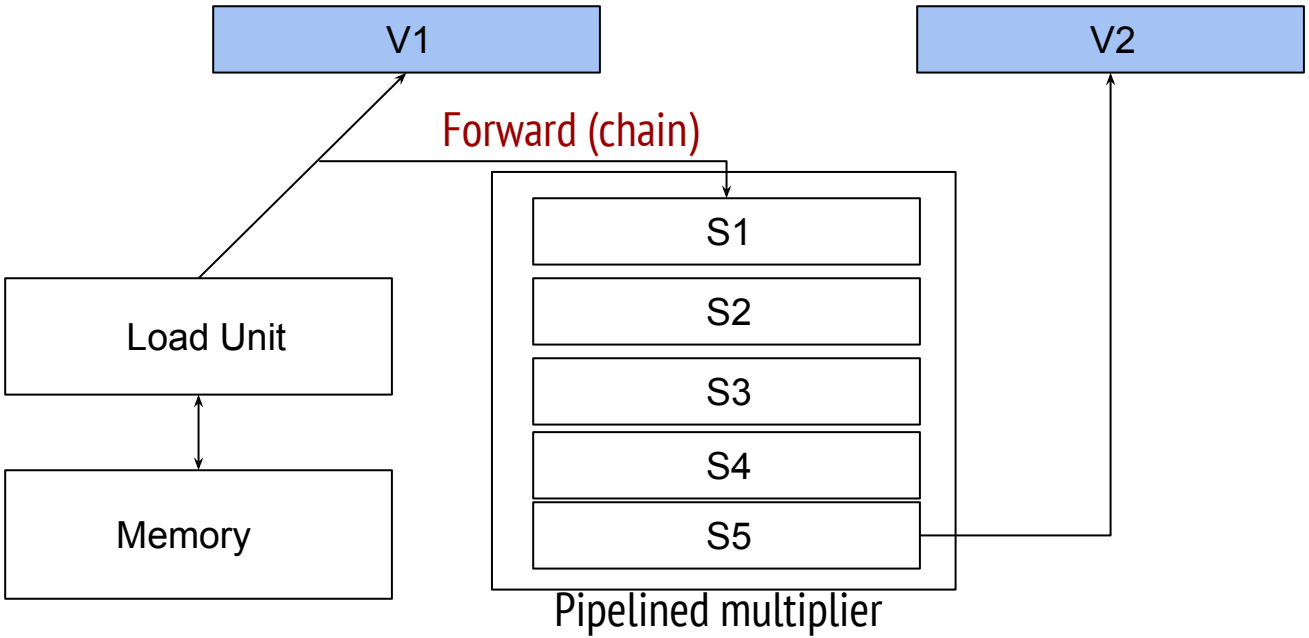

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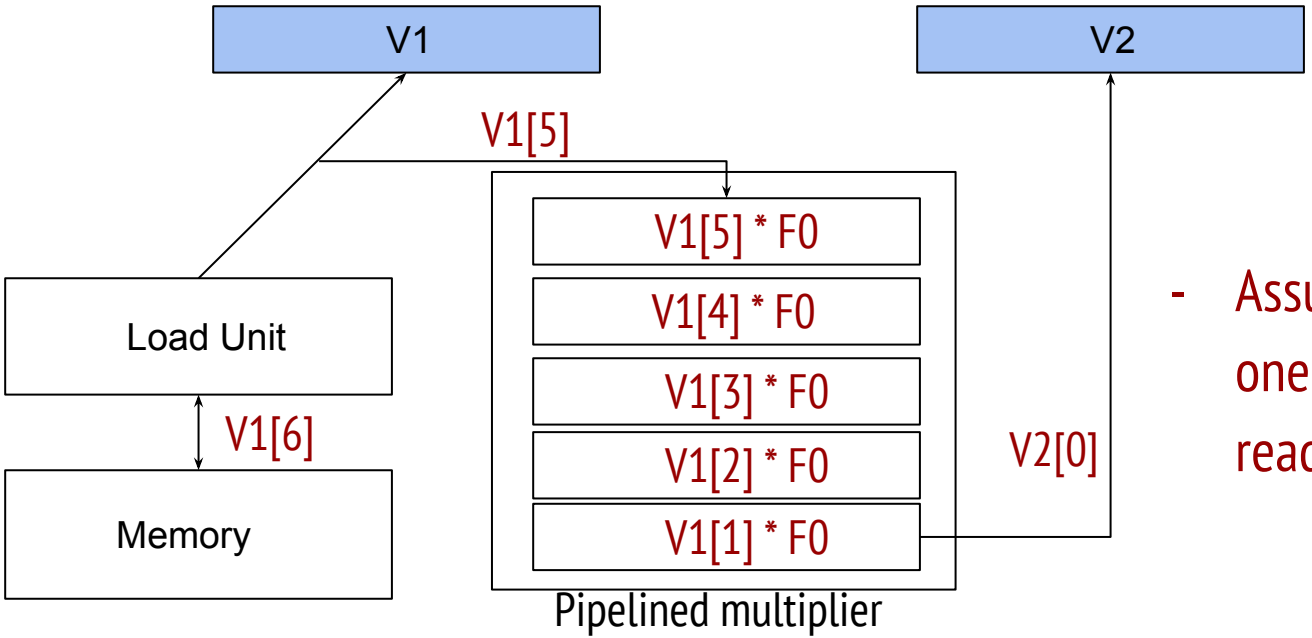

- Assuming single lane, one element in V2 is ready in each cycle

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- How data forwarding works between dependent instructions? Chaining techniques used to forward data