Computer Architecture

Memory Hierarchy

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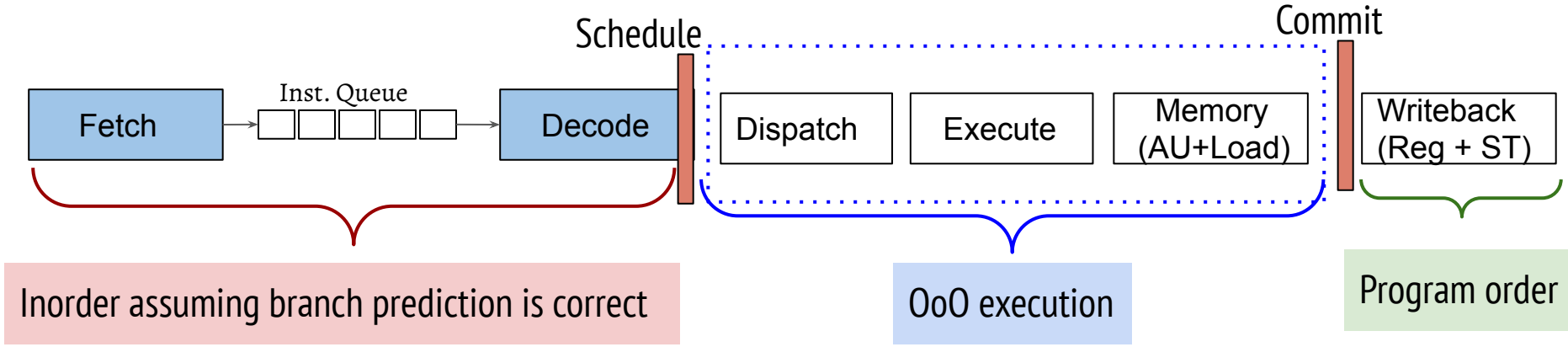
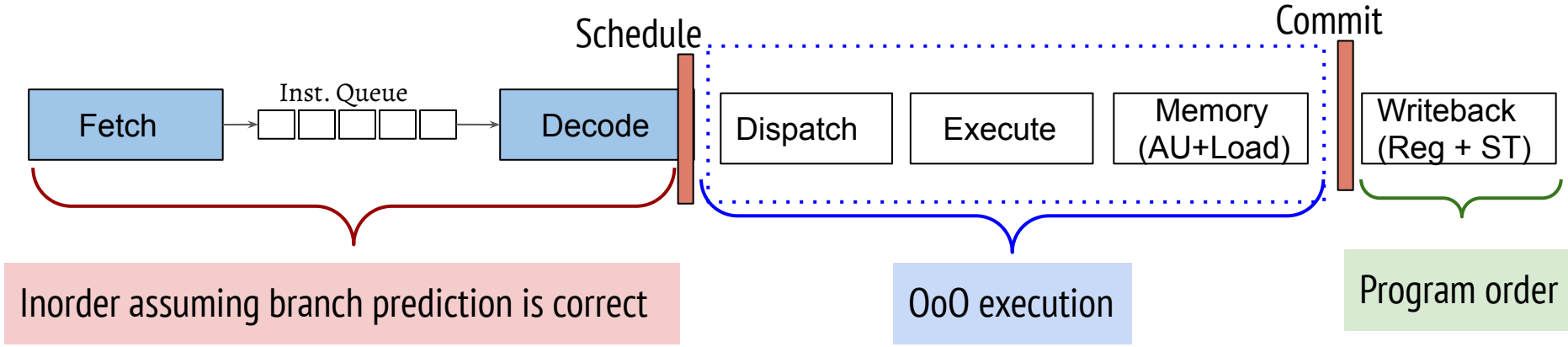
Superscalar Frontend and Memory Interactions



- What are the memory operations in each phase?
- How much delay can be tolerated?
- Implications of memory access bottleneck?

Superscalar Frontend and Memory Interactions



- Operation: Instruction (load)
- At any point of time #of instructions >= issue width
- Resource underutilization, pipeline stall ⟶ reduced IPC

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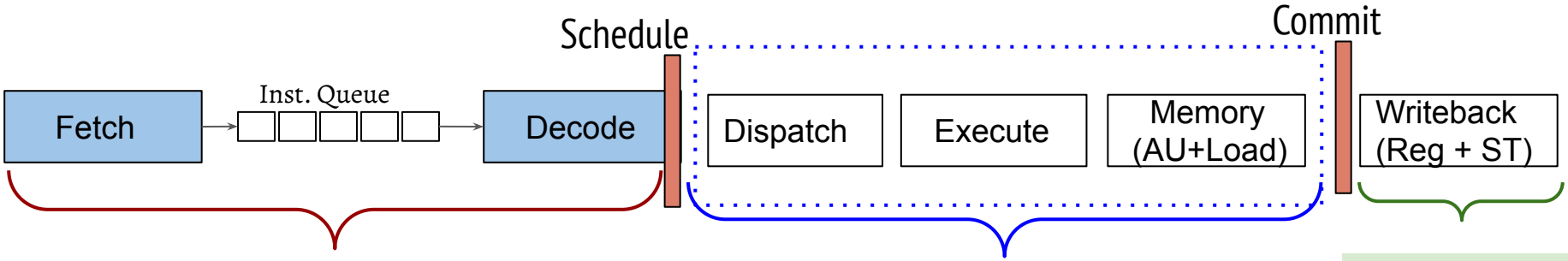

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- Operation: Data (load)
- No FU is idle when there are instructions in the corresponding reservation station
- RS and/or ROB full ⟶ Stall ⟶ Reduced IPC

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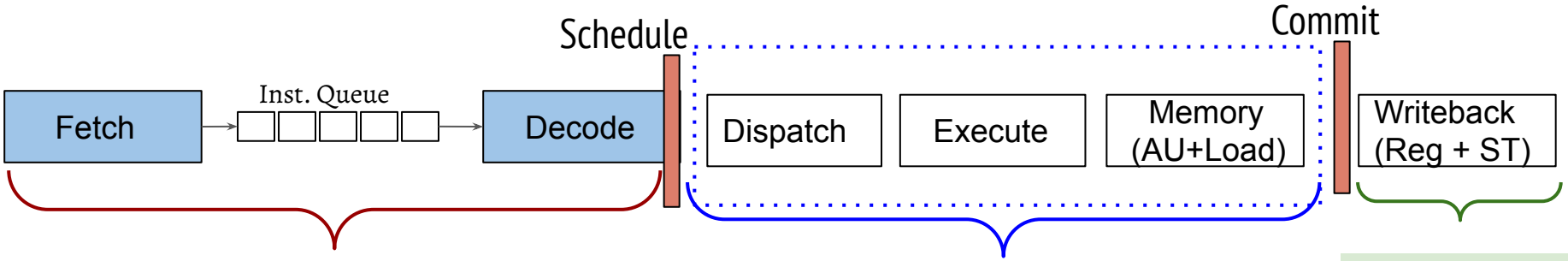

- Operation: Instruction (load)
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- Operation: Data (load)
- No FU is idle when there are instructions in the corresponding reservation station
- RS and/or ROB full ⟶ Stall ⟶ Reduced IPC

- Operation: Data (store)
- No instructions are waiting to be committed because of a leading store
- ROB full ⟶ Stall ⟶ Reduced IPC

Why not use only registers?

Memory Type	Approx. # of transistors required to store one bit	Access time	Usage
Flip-flop	20	Fast	Registers
SRAM	6	Medium	Cache and Registers
DRAM	1 (+1 capacitor)	slow	Primary Memory

- Faster is more costly because more #of transistors, less storage density, more power
- If money is not an issue, why not design my storage entirely using SRAM?

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- If money is not an issue, why not design my storage entirely using SRAM?
  - Access latency increases with size

Typical Memory Hierarchy

Memory Element	Typical Capacity	Access time
Register File	~1KB	0.3 ns
L1 Cache	64KB	1ns
L2 Cache	256KB	3ns - 10ns
L3 Cache	2MB - 4MB	10ns - 20ns

- As much as possible, serve the data from the levels closer to the processor

Common Terminologies (Recap)

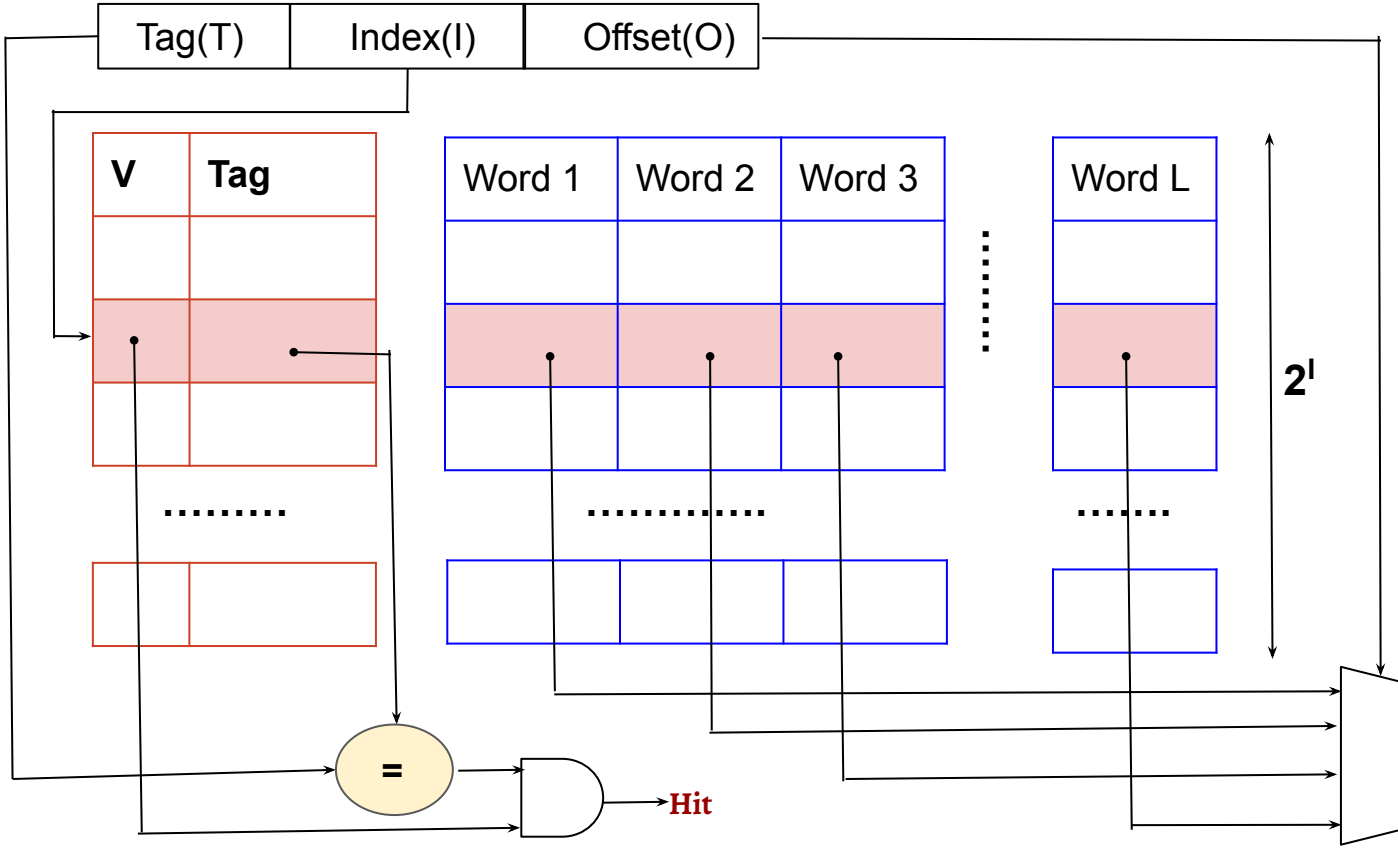
Program execution

- Access locality
- Working set
- Types of access
- Addressing
- Cache hit
- Cache miss

Mechanisms and Policies

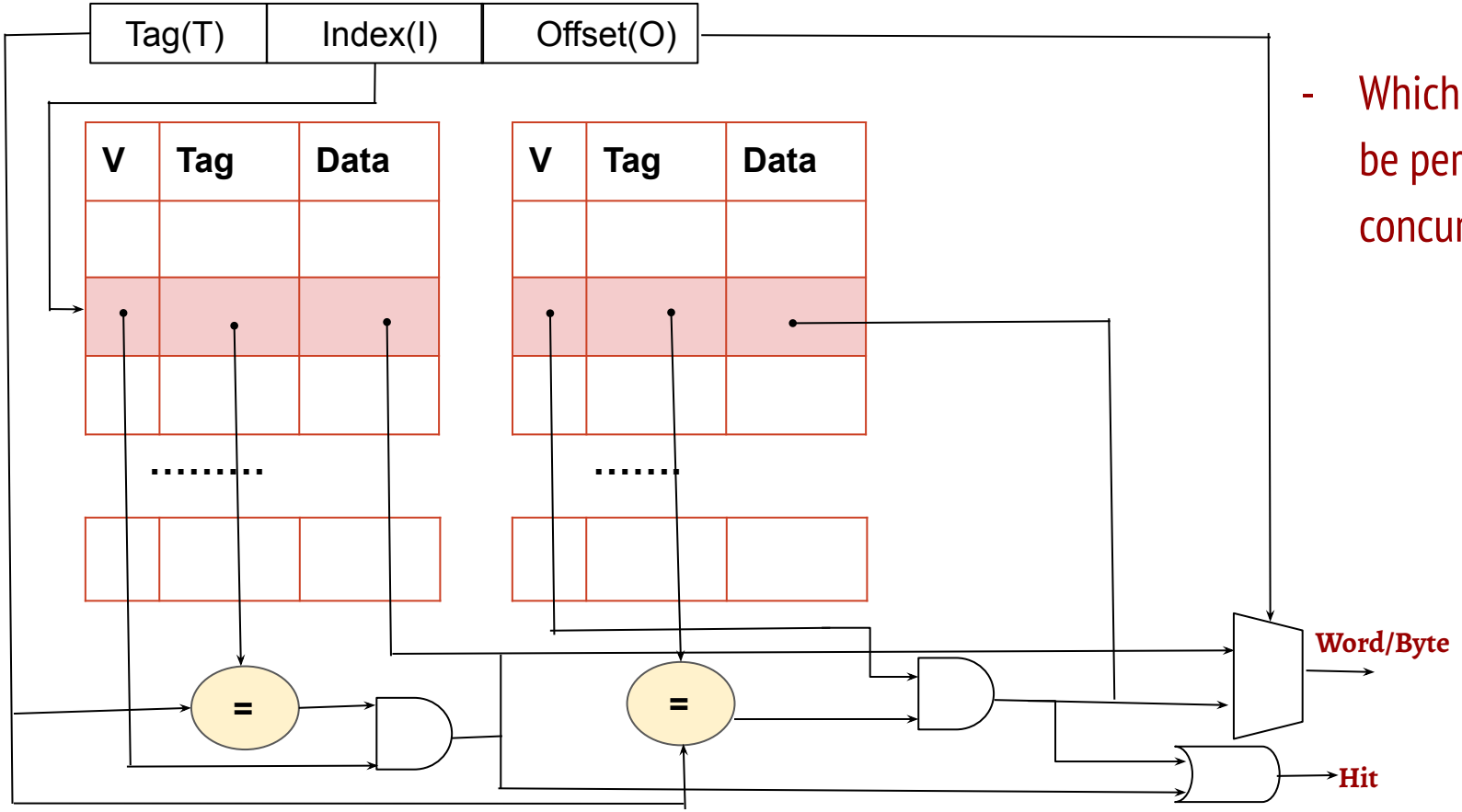
- Cache blocks
- Block placement: direct mapped, set-associative, fully associative
- Block Identification: index, tag, valid bit,
- Block replacement policies
- Write strategy: write-through, write-back, dirty bit, write allocate

Direct-mapped Cache



- Valid bit
- Dirty bit?
- Design parameters
  - Block size
  - Cache size
  - Mapping function
  - Index bits
  - Tag bits

2-way Set Associative Cache



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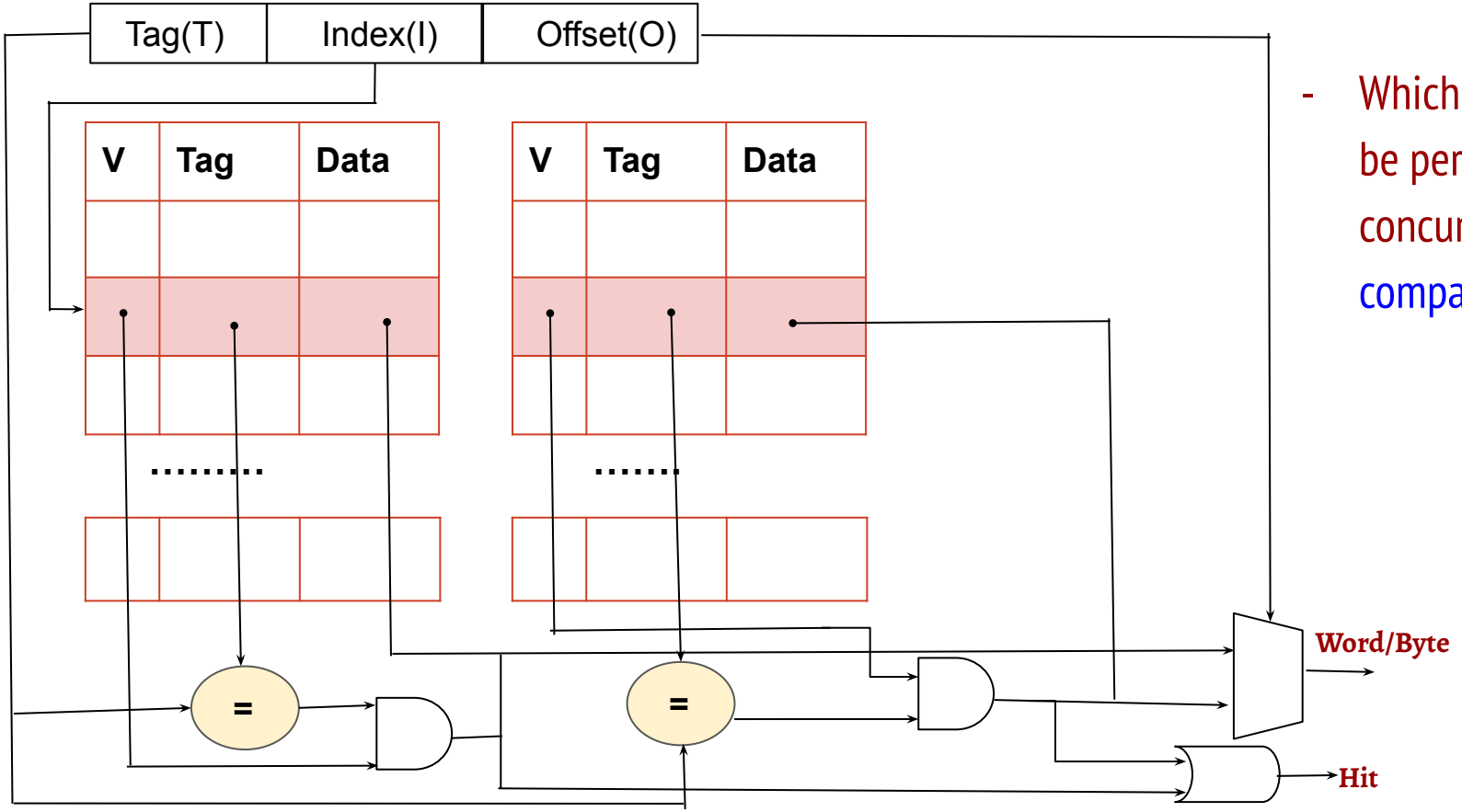
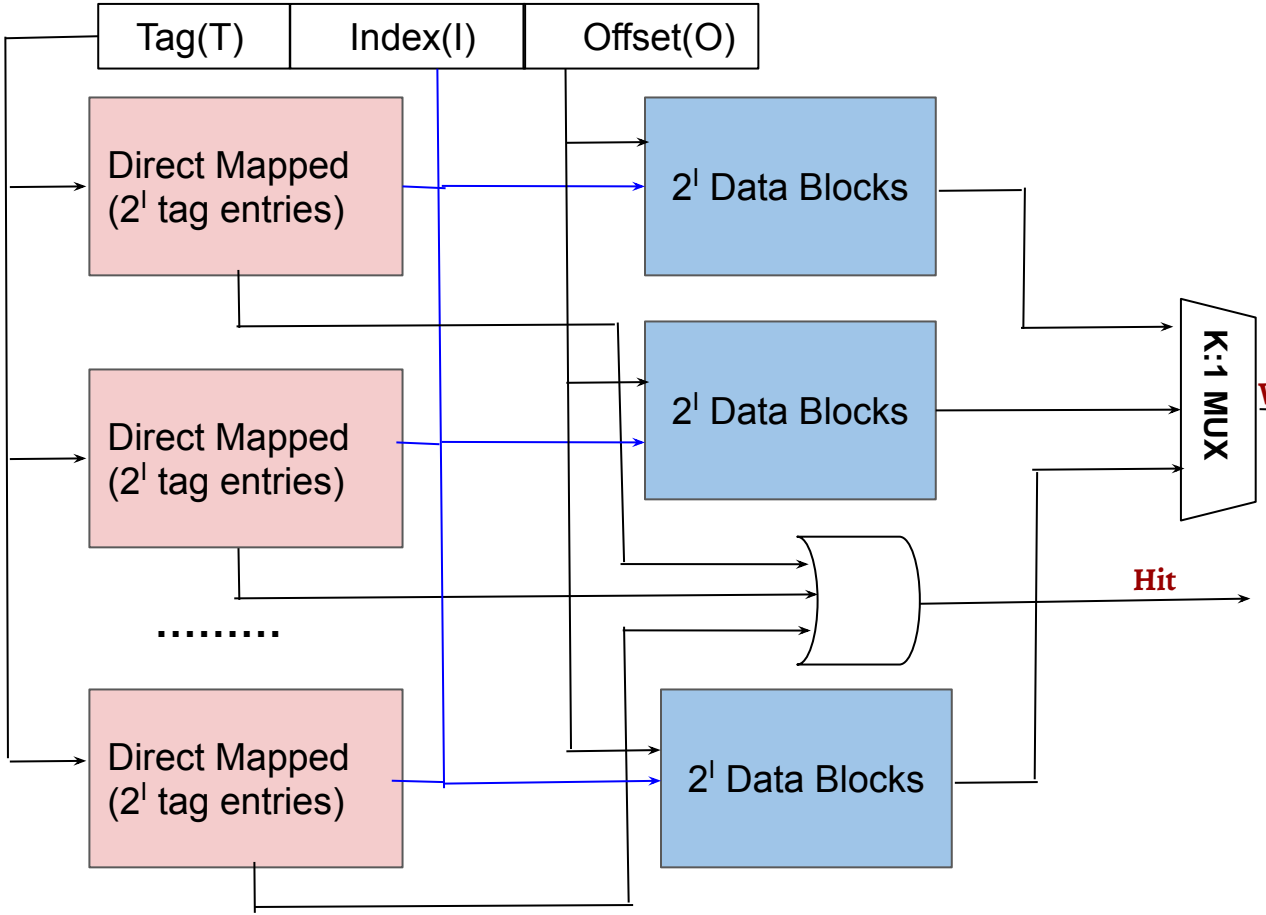


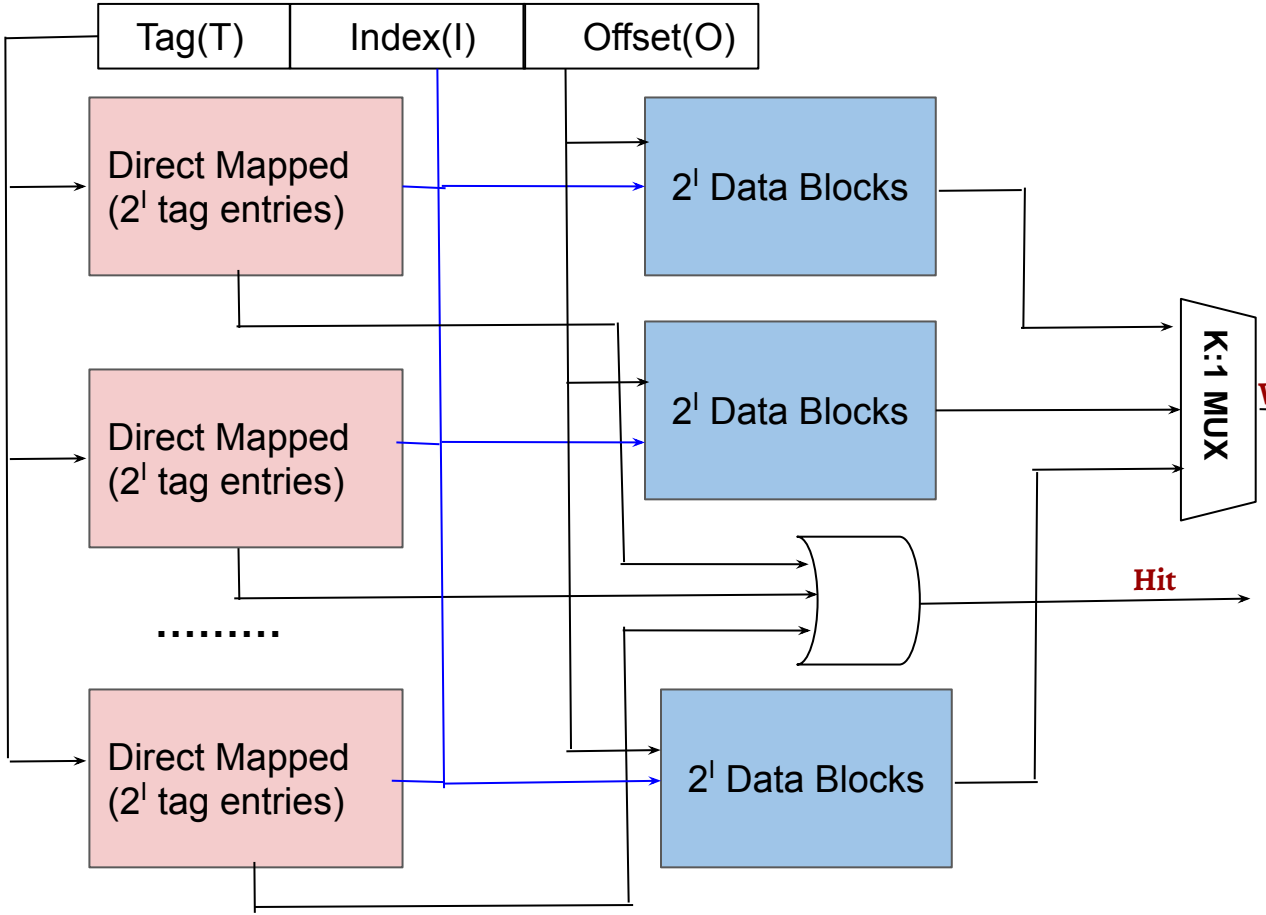
- Which operations can be performed concurrently? Tag comparison, data read

K-way Set Associative Cache



- What should be the value of K?
- What factors determine the limits on K?
- Cache replacement policies (LRU, FIFO ...)
- RRIP, Jaleel et al. (paper review due next week)

K-way Set Associative Cache



- What should be the value of K? Larger the K, more is the hit latency
- What factors determine the limits on K?
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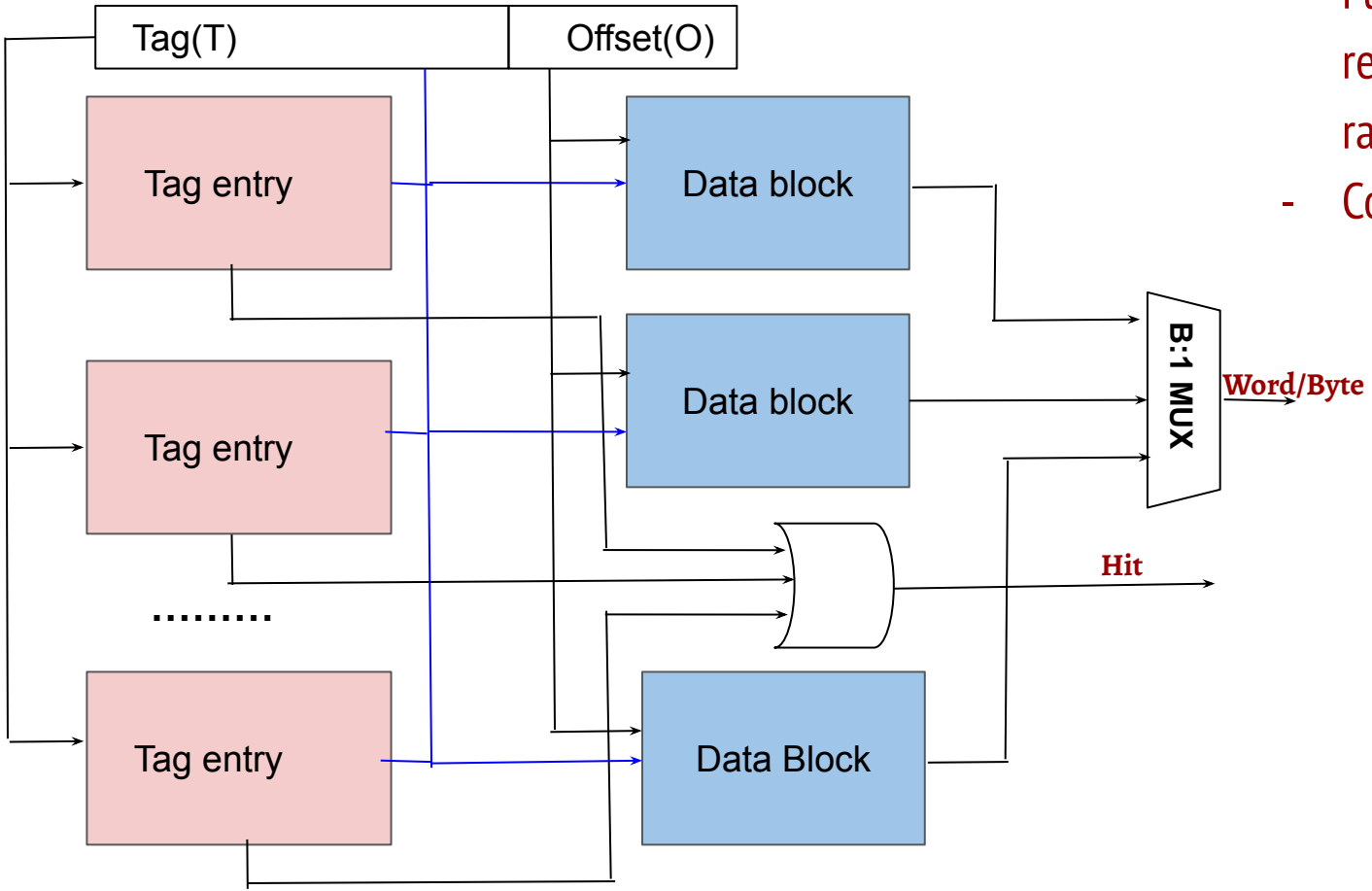
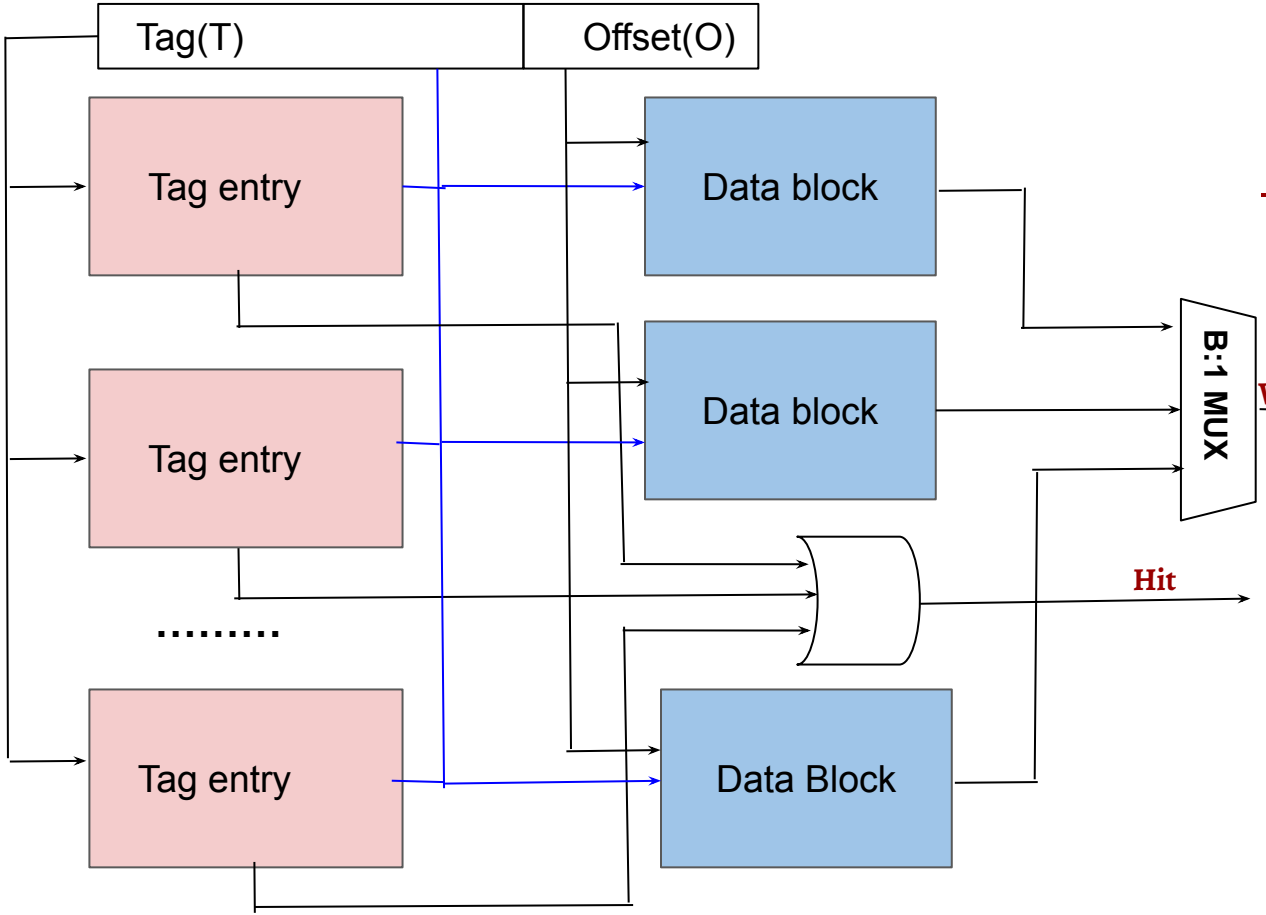
Fully Associative Cache



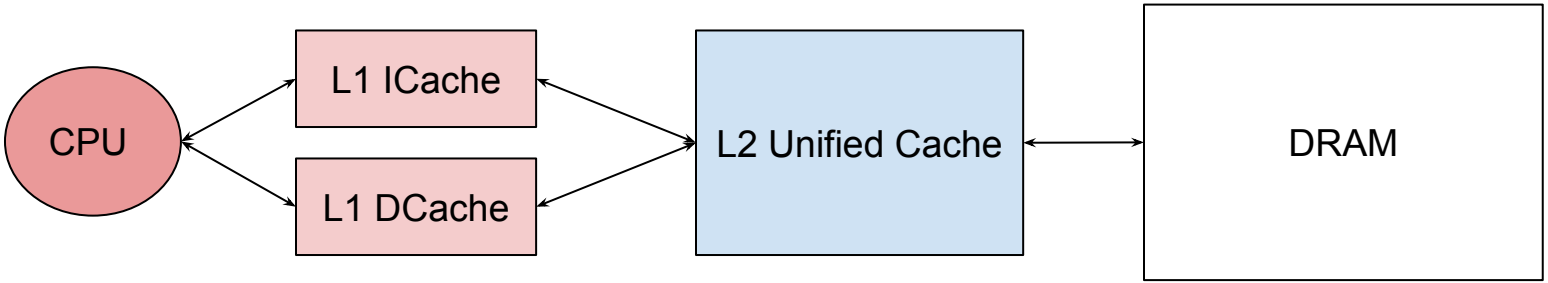
- Fully associative cache results in lowest miss rate (True/False)
- Cost vs. Benefit?

Fully Associative Cache



- Fully associative cache results in lowest miss rate (True/False)
- Cost vs. Benefit? Increasing associativity after a point return on cost is diminished

Multi-level Caches



- Why design a multi-level cache, why not a single big cache?
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- How to handle write operations?
- What are the metric of interest?
- Is there any need for bypassing certain levels of caches?

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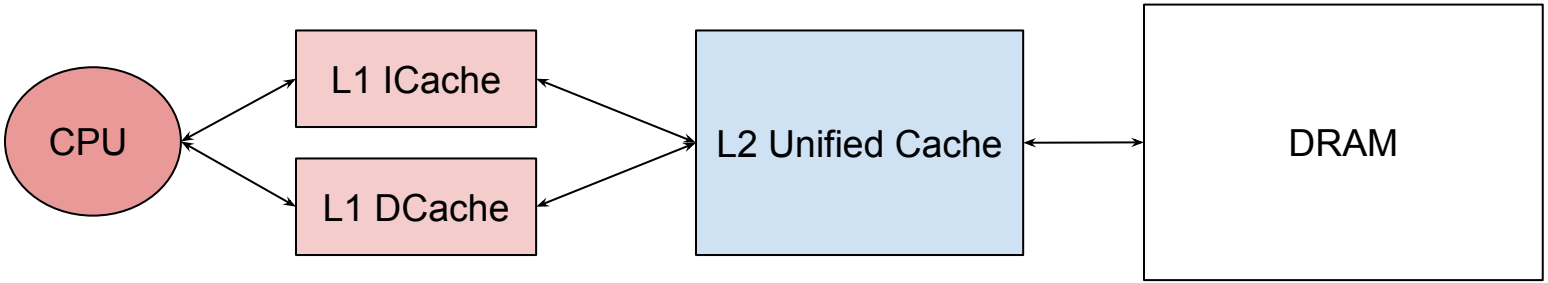

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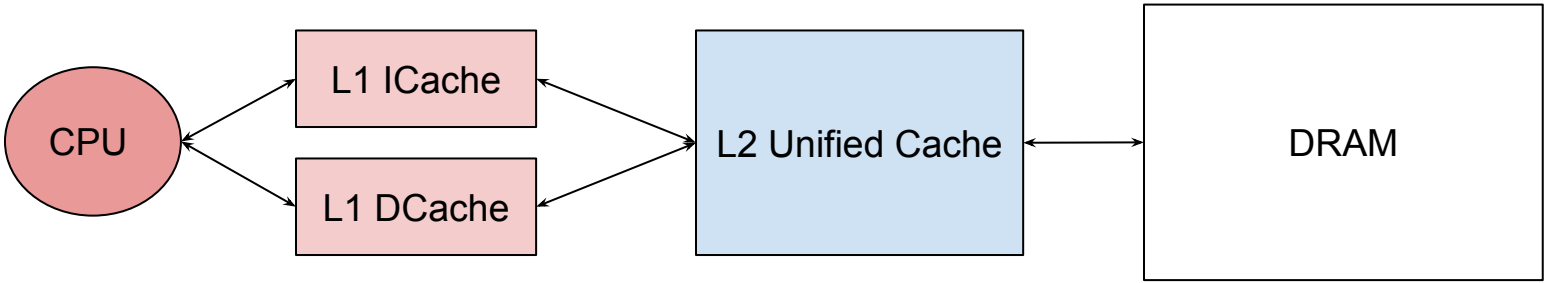

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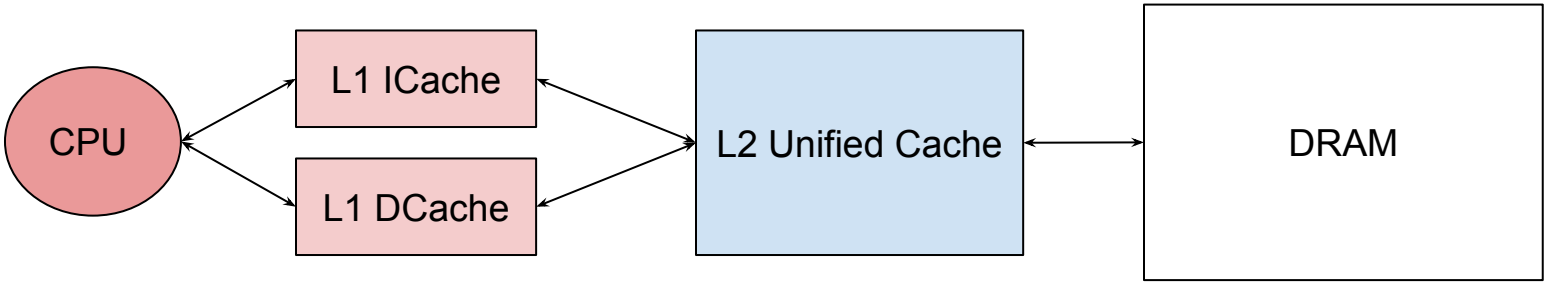

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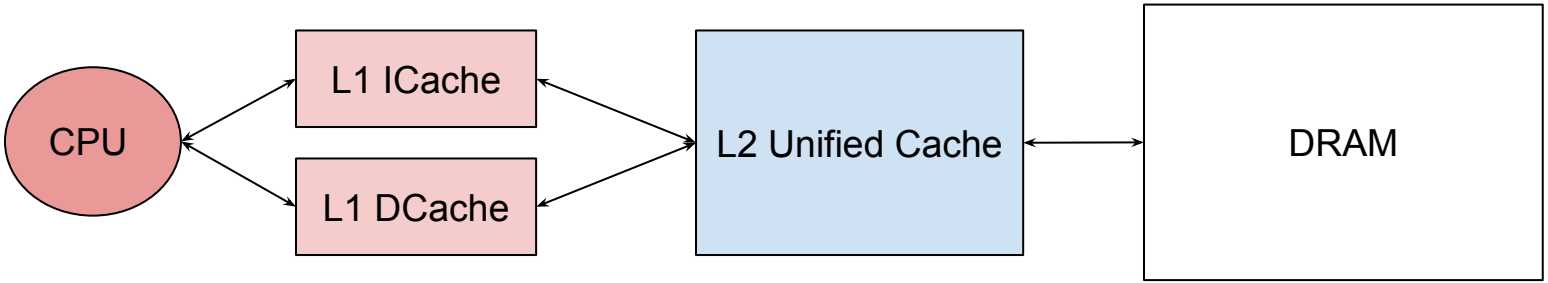

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- How to handle write operations? Cache hit: write through vs. write back, Miss: Write allocate
- Is there any need for bypassing certain levels of caches? Page table updates, I/O (MMIO)
- What are the metric of interest?

Metrics related to cache

- Local miss rate = # of misses / # of accesses to the cache
- Global miss rate = # of misses / Total # of memory accesses
- Misses per instruction = # misses / # of instructions (misses per Kilo instruction MPKI)

- Avg. memory access time (AMAT) = Hit time + Miss Rate * Miss Penalty
- AMAT (for two levels) = Hit time + Miss Rate $_1$ * Miss Penalty $_1$ + Miss Rate $_2$ * Miss Penalty $_2$

Classifying cache misses

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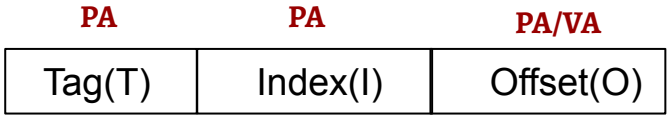
- How to measure? Total cache misses in k-way set associative cache - # of misses in fully associative cache
- How to reduce? Increased associativity, cache prefetching?

Cache Types (Mapping)



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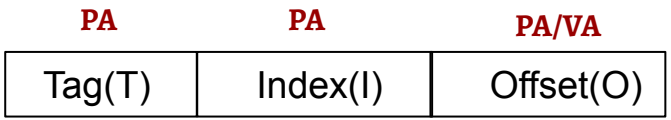
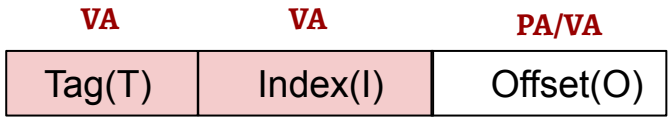


- Physically indexed and physically tagged (PIPT)
- Advantages/disadvantages? Independent of virtual address space. Issue: cache OP possible only after address translation



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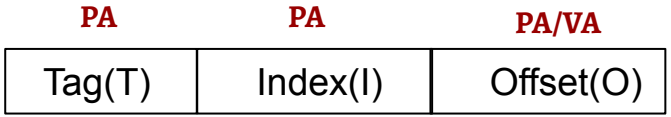

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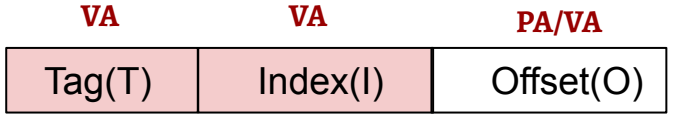

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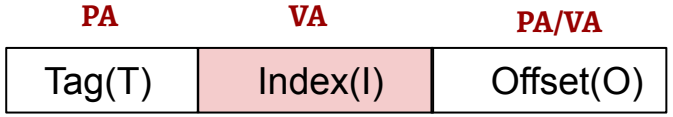

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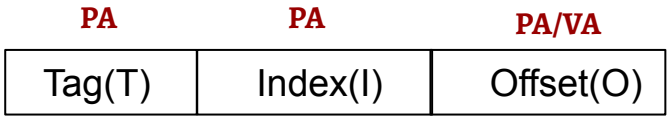

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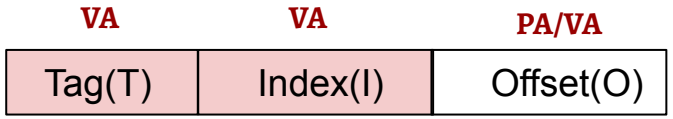

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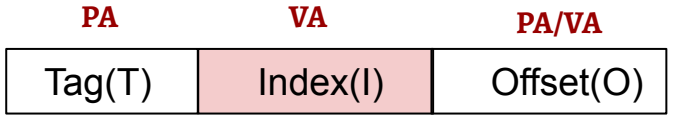

- Virtually indexed and physically tagged (VIPT)
- Data read can start after index mapping. Page size depends on block size and # of index bits