CS698Y **Name:** _____
End-term (Quiz 2.0)
19th November, 2017
Time Limit: Maximum 180 Minutes **Roll No.:** _____

This exam contains 13 pages and 10 questions. Maximum points: 100

Tips:
Be concise and cognizant.
There will be penalty for verbosity.
Do not spend too much or too little time on any particular question.

Points Table (For the Instructor only)

Question	Points	Score
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
9	10	
10	10	
Total:	100	

"I promise I will write this exam honestly and ethically"
Your Signature:

1. (10 points) There are different possible DRAM addressing modes as discussed in one of the lectures. However, there is no single addressing mode that can benefit all kinds of access patterns. Your job is to come up with a DRAM address mapping scheme that can improve bank-level-parallelism, row-buffer-locality, and can equally benefit stream based applications and pointer-chasing applications.

2. (10 points) As discussed in one of the lectures, row conflicts are costlier than row hits. So it would be good to have an adaptive policy that can decide when to use an open page policy and when to use a closed-page one. Explain how will you design such an adaptive policy so that all accesses will be serviced with ACT and CAS only and no RP.

3. (10 points) It would be great to have a processor that can operate on compressed data so that data will be compressed at the DRAM and all the caches will store the compressed data, transfer compressed data, and processor will perform computation on compressed data. Explain the relevant challenges that you may encounter while designing such a system.

4. (10 points) Biswa wants to design a hypothetical 27D (3×3×3D) memory system where three faces of the Figure shown at the top, can have L3/DRAM cache, DRAM chips, and a Processing in Memory framework, respectively. Discuss the challenges and solutions to realize this kind of memory system.

5. (10 points) DVFS controllers at the Memory and CPU, control voltage and frequency of each core and memory controller. One of the major issue with this technique is it limits the peak bandwidth of a DRAM device. Design a DVFS controller that can still provide full bandwidth to/from the DRAM.

6. (10 points) Weighted speedup and Harmonic mean of speedups are two widely used metrics that quantify throughput and fair performance. Please provide a scenario where you feel these metrics conclude wrongly. You can take a case study as DRAM scheduling or any cache optimizations.

7. (10 points) What did you learn from PA1, PA2, RA1, and RA 2.x (Any specific skills) ? Which one (PA or RA) you liked the most and why?

Algorithm 1: **Square-and-Multiply Exponentiation**

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1: Input: Base B, Exponent E (e_{n-1} .....e_0), and Modulo M
2: Output: B^E mod M
3: R = 1
4: for all i, from n-1 to 0 do
5:    R = SQUARE (R)
6:    R = MOD (R, M)
7:    if (e_i)==1 then
8:       R = MUL (R, B)
9:       R = MOD (R, M)
10: return R
```

8. (10 points) On a two core system, a spy application is running on core-0 and and the above algorithm is running on core-1. The spy can mount an evict+reload side-channel attack at the LLC and infer about the 1s and 0s that are present in the exponent. Explain in what way the spy can infer about the 1s and 0s? Also, provide an attack strategy assuming LLC is non-inclusive or exclusive of private caches.

9. (10 points) During RA 2.2, Nayan presented about the Processing in Memory (PIM). Biswa wants to have processing power nearer to each LLC bank and call it as Processing in Cache (PIC). Provide design choices that you would like to keep in mind while designing PIC.

10. (10 points) What did you like/hate the most about this course and why? Similarly, what did you like the most and hate the most about BIswa and why? Overall how is CS698Y with Biswa?