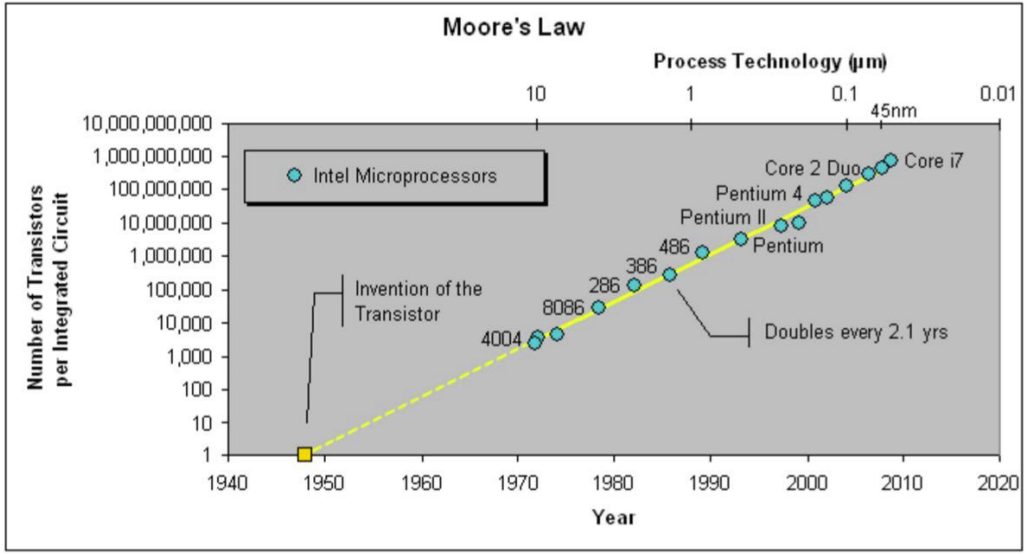
3D/2.5D DRAM stacking

RA2.2 by Shubham Aggarwal

Moore's Law



https://fossbytes.com/moores-law-is-finally-dead-rest-in-peace-moores-law/

Number of **Transistors on chip** doubles after every 2 years. **How?**

Limits to Moore's Law

How can you cheat the size of atom?

- Mike Mayberry, VP Technology and Manufacturing Group **Intel (5/2013)**
  - .. has looked down the highway of conventional silicon development and reckons things become foggy beyond about the **7-nm node**

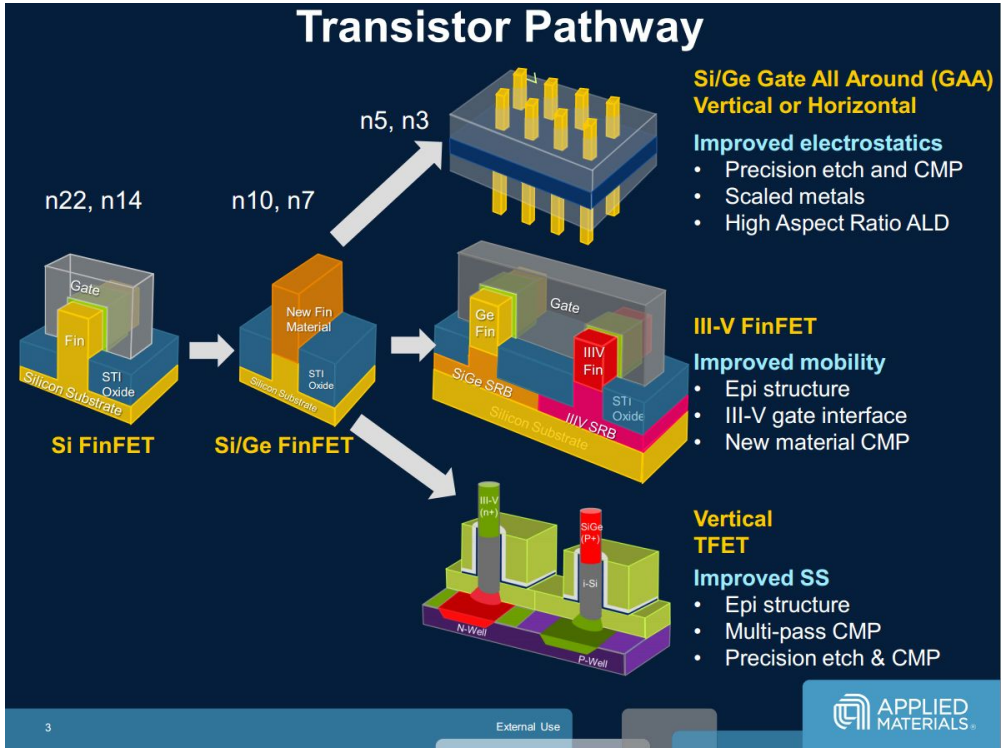
  < http://www.eetimes.com/electronics-news/4414897/More-varied-research-needed-says-Intel >
- The end of Moore's Law is on the horizon, says **AMD (4/2013)**
  - Gustafson, chief graphics product architect at AMD, claimed "You can see how Moore's law is slowing down"

    http://www.zdnet.com/amd-sees-the-era-of-moores-law-coming-to-a-close-7000013413/

http://slideplayer.com/slide/5941243/

How can you increase more transistors on chip since 14nm seems to be the final node for silicon?

Possible Solutions



Other Materials like

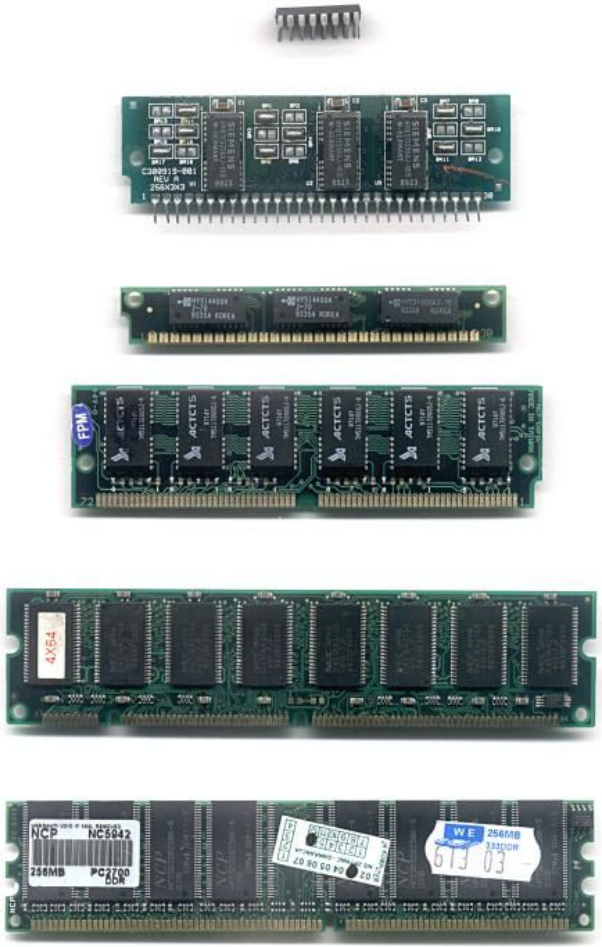
SiGe(7nm)

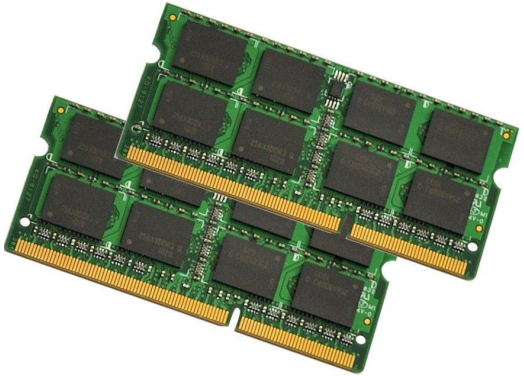
Ge(3-5 nm)

But they will also stop at one point.

https://www.extremetech.com/computing/162376-7nm-5nm-3nm-the-new-materials-and-transistors-that-will-take-us-to-the-limits-of-moores-law

Increase the area to accumulate more transistors or the slots in machine(off-package DRAM)

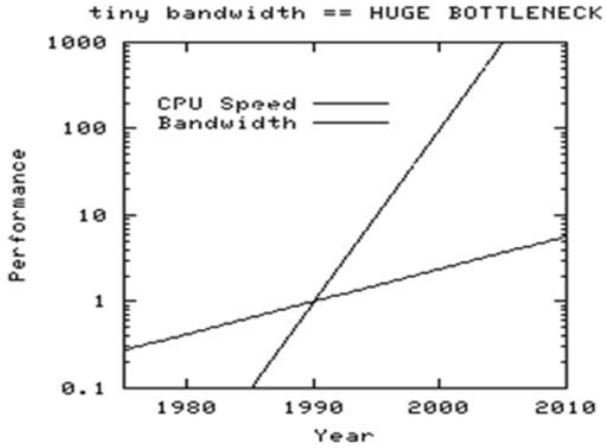




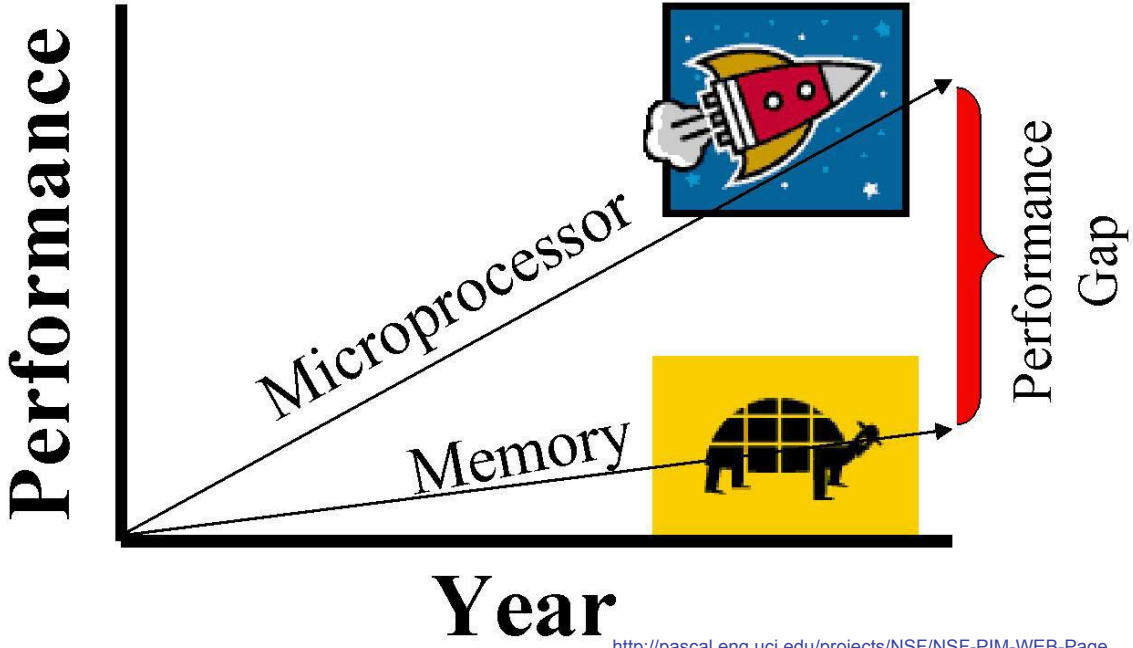
https://en.wikipedia.org/wiki/Dynamic_random-access_memory

http://www.alphr.com/features/391525/how-to-find-ram-speed-size-and-type

What about Memory wall and Bandwidth wall?



http://en.community.dell.com/techcenter/high-performance-computing/w/wiki/2284

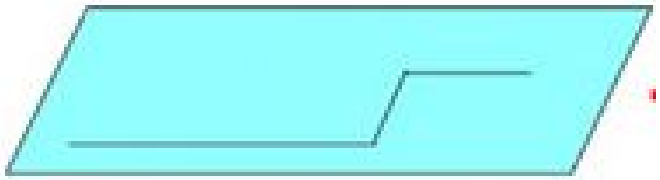


http://pascal.eng.uci.edu/projects/NSF/NSF-PIM-WEB-Page

https://i.ytimg.com/vi/I_nRj6-ZKhs/maxresdefault.jpg

https://i.ytimg.com/vi/gV3MIKIcS0I/hqdefault.jpg

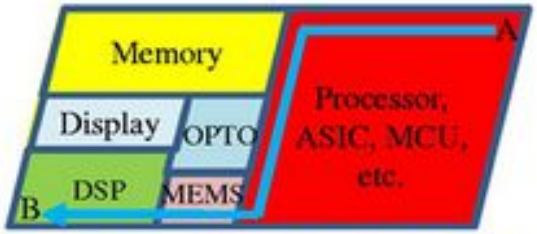
Interconnect delay



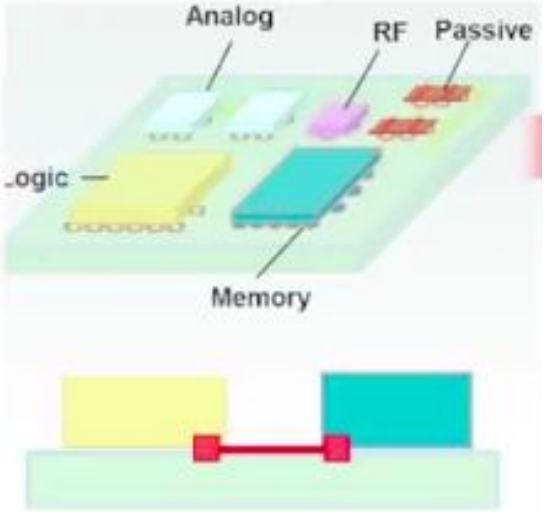
2D Routing (large chip)

Moore's law

2D SoC

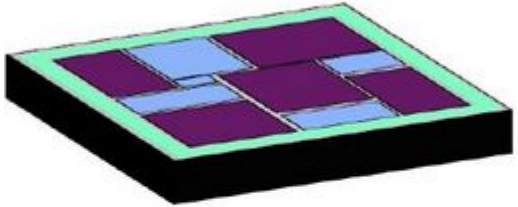


Long wiring (from A to B) in 2D SoC



Flipchip + wire bond

SOC Node N



Digital Logic, SRAM

Analog functionality

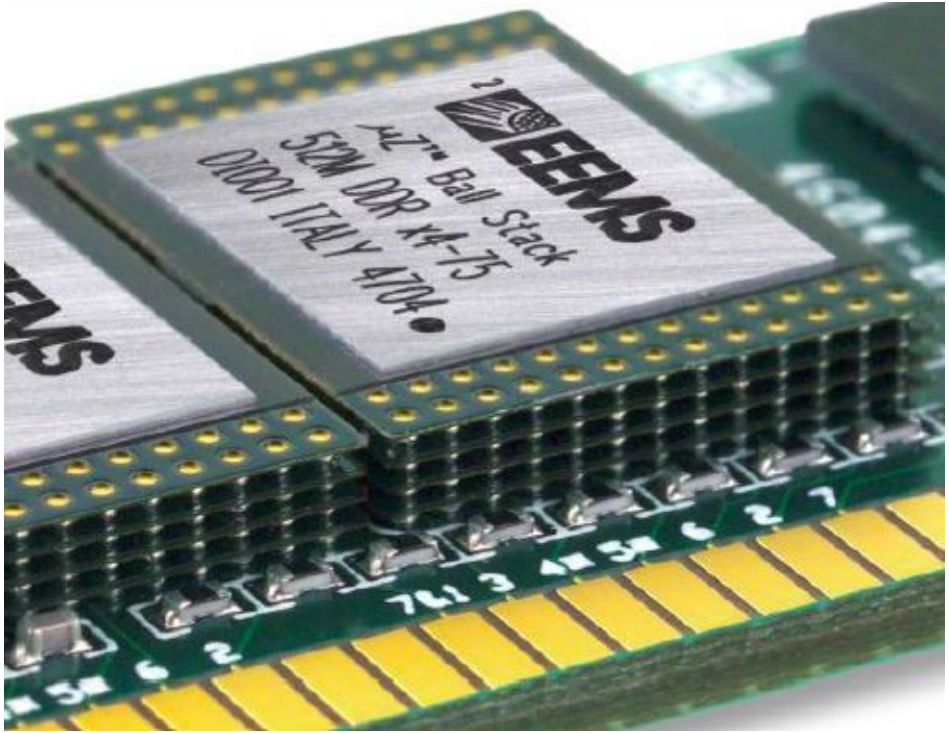
I/O drivers

Die stacking by Yuan Xie and Jishen Zhao

http://semiconductortechnology.blogspot.in/2014/03/global-3d-ic-and-tsv-interconnect.html Stanford university

Time to switch to 2.5D or 3D DRAMs

- Low Cost
- Small Space
- Low Power
- Wide Bandwidth
- Shorter Interconnect/ Latency Improvement
- Heterogeneous integration



www.google.com

Understanding 3D

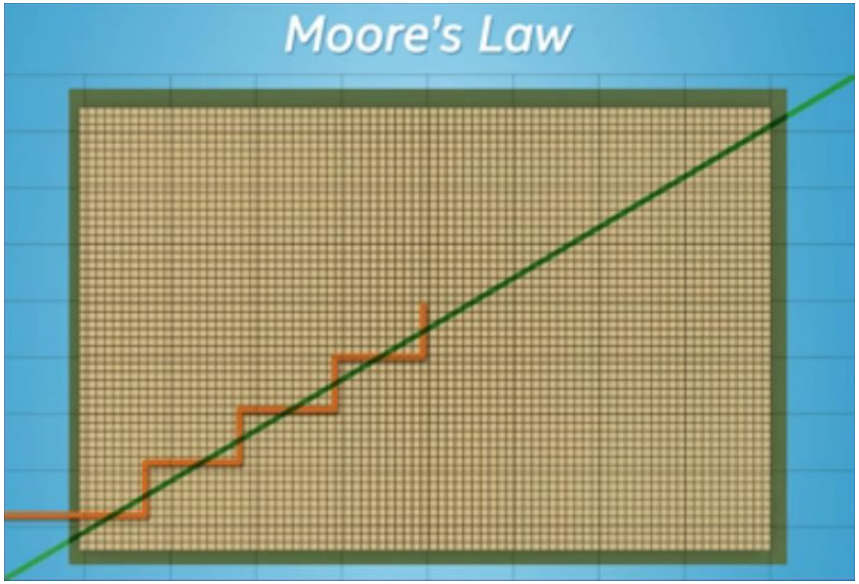
www.google.com

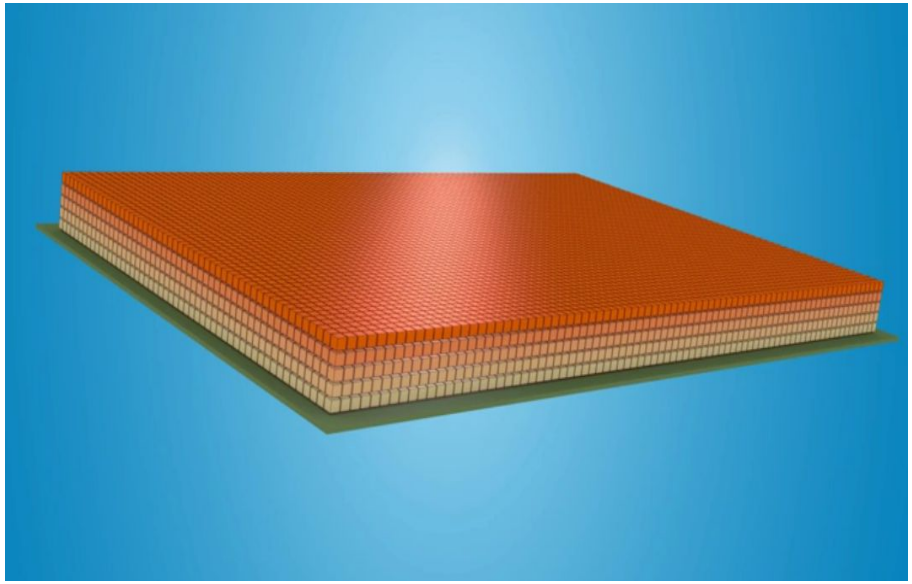
A Villa is a memory cell

A Room in a Floor is a memory cell

What can be said about population density?

Similarly

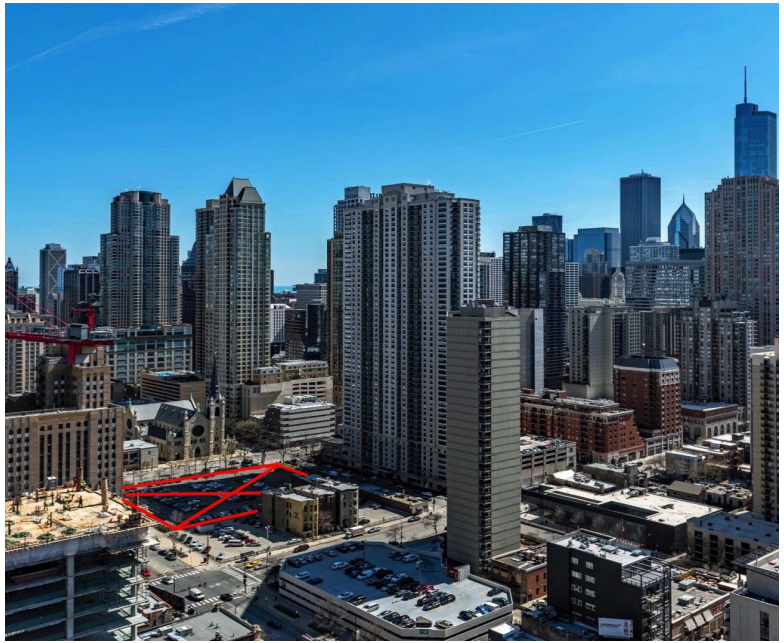




www.intel.com

Understanding 2.5D and 3D

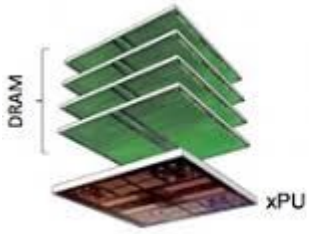
Mumbai



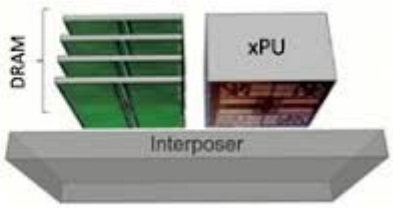
Chicago

www.google.com

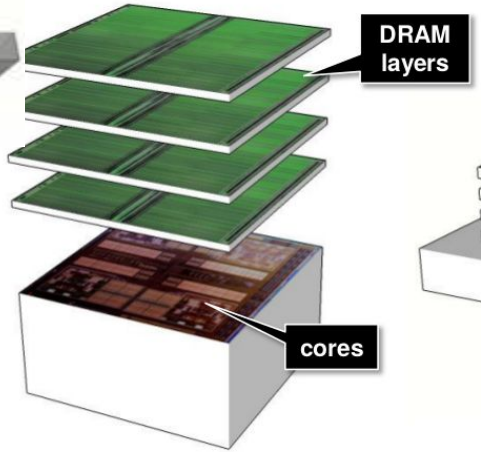
Similarly



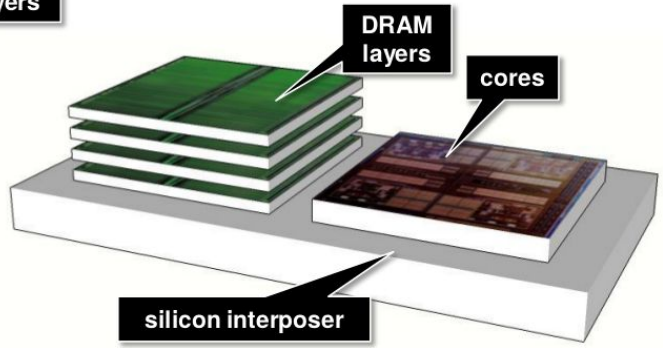
VERTICAL STACKING (3D)



INTERPOSER STACKING (2.5D)



"Vertical"

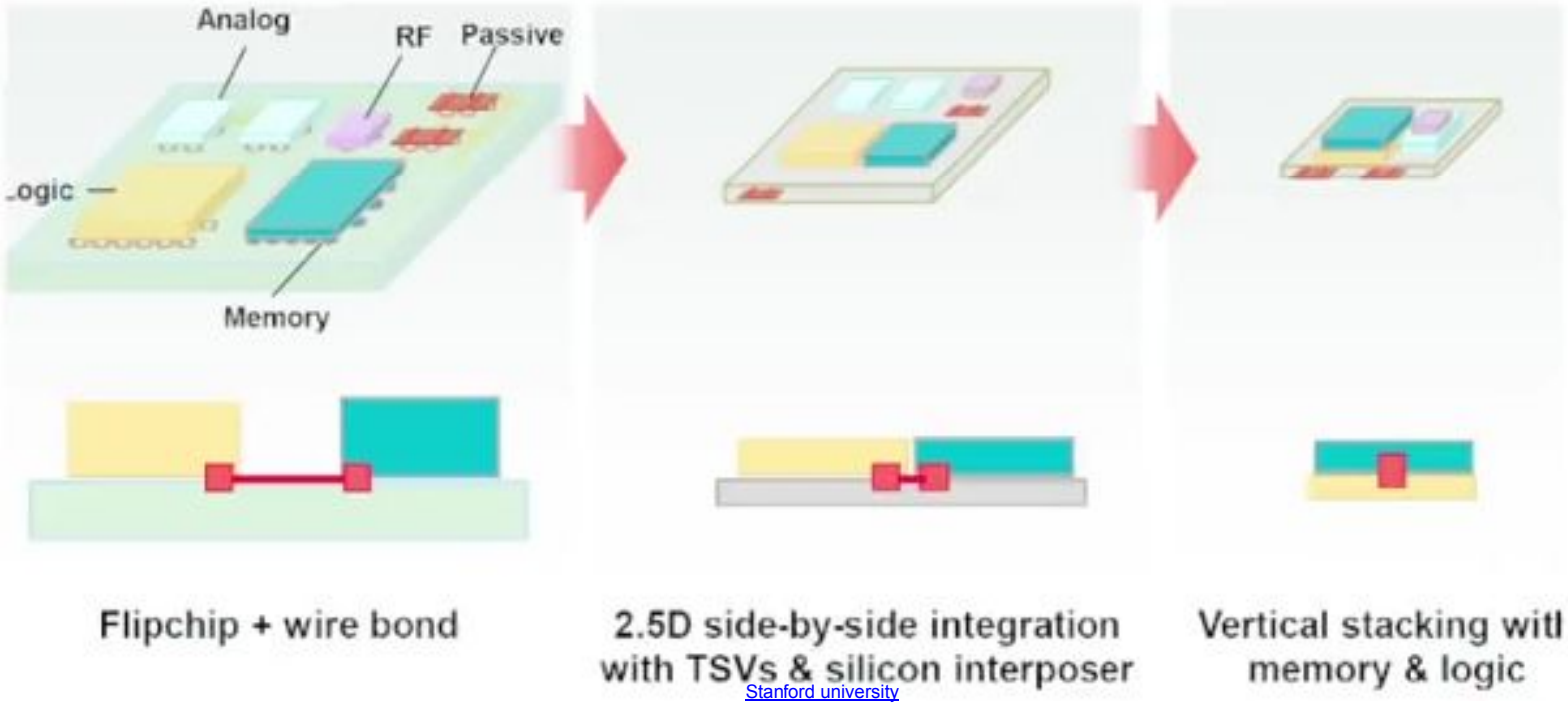


"Horizontal"

256 MB

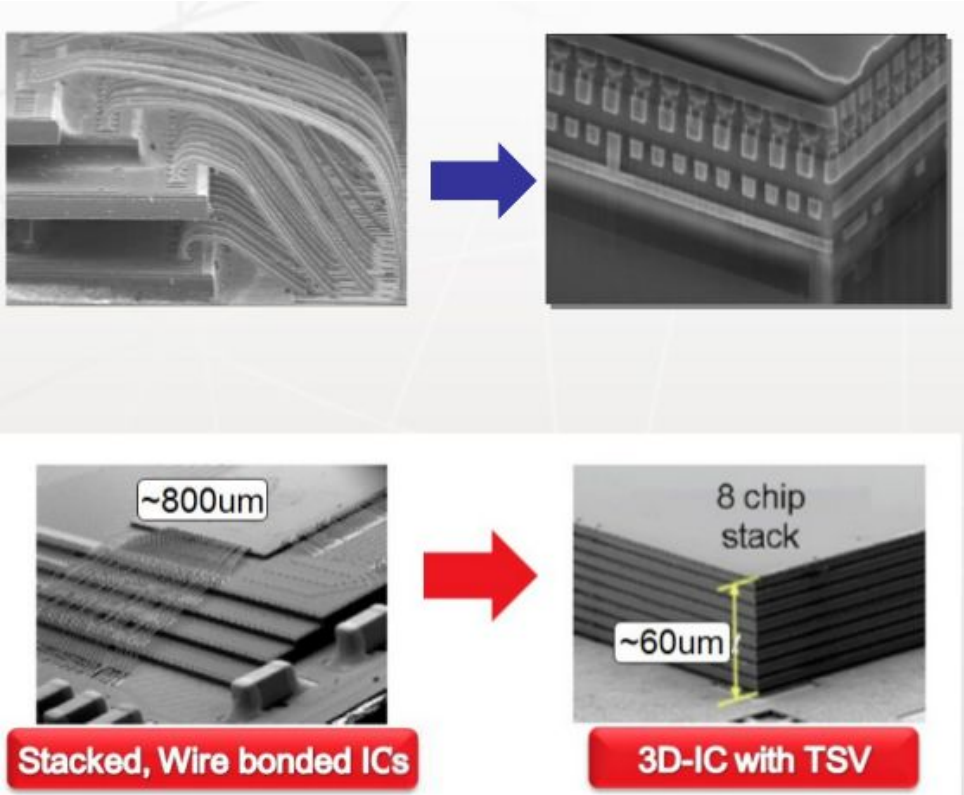
Samsung @ ISSCC'11: "A 1.2V 12.8Gb/s **2Gb** Mobile Wide-I/O DRAM with 4x128 I/Os Using TSV-Based Stacking"

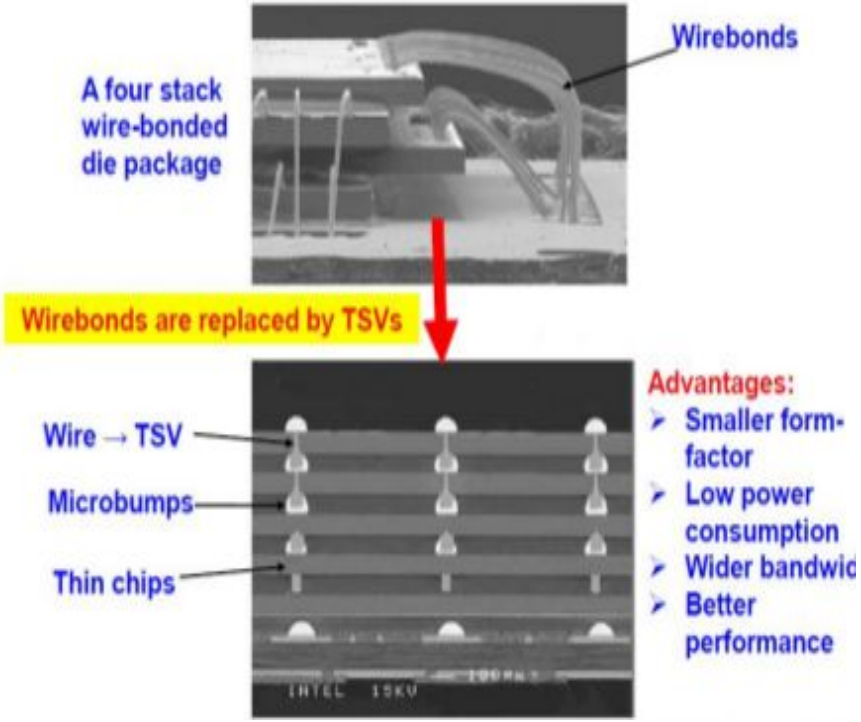
2D vs 2.5D vs 3D



Stanford university

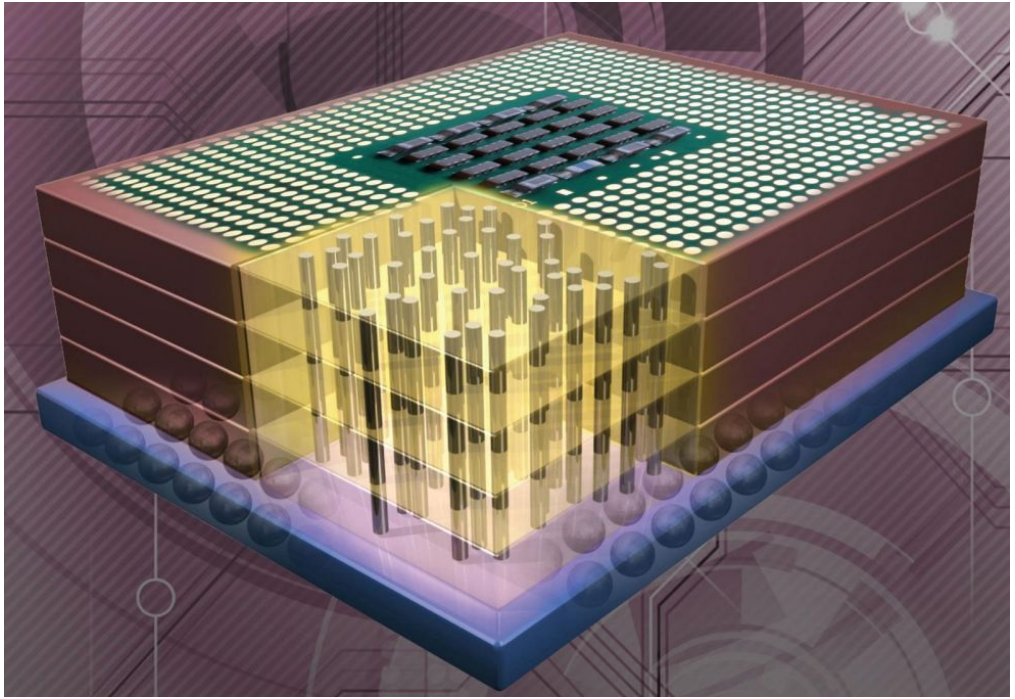
Stacking





whatis.techtarget.com/fileformat/TSV-Tab-separated-values-file

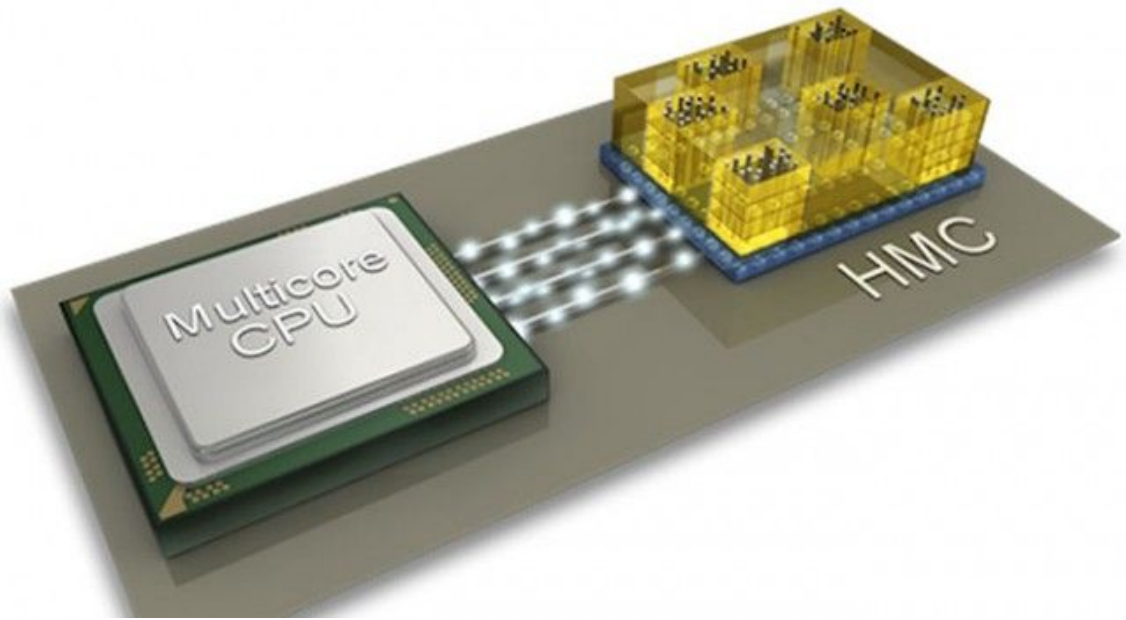
Through Silicon Via(TSV)



http://www.linx-consulting.com/TSV2012.html

Pillars of a building or electric wires for sockets of a building.

Interposer

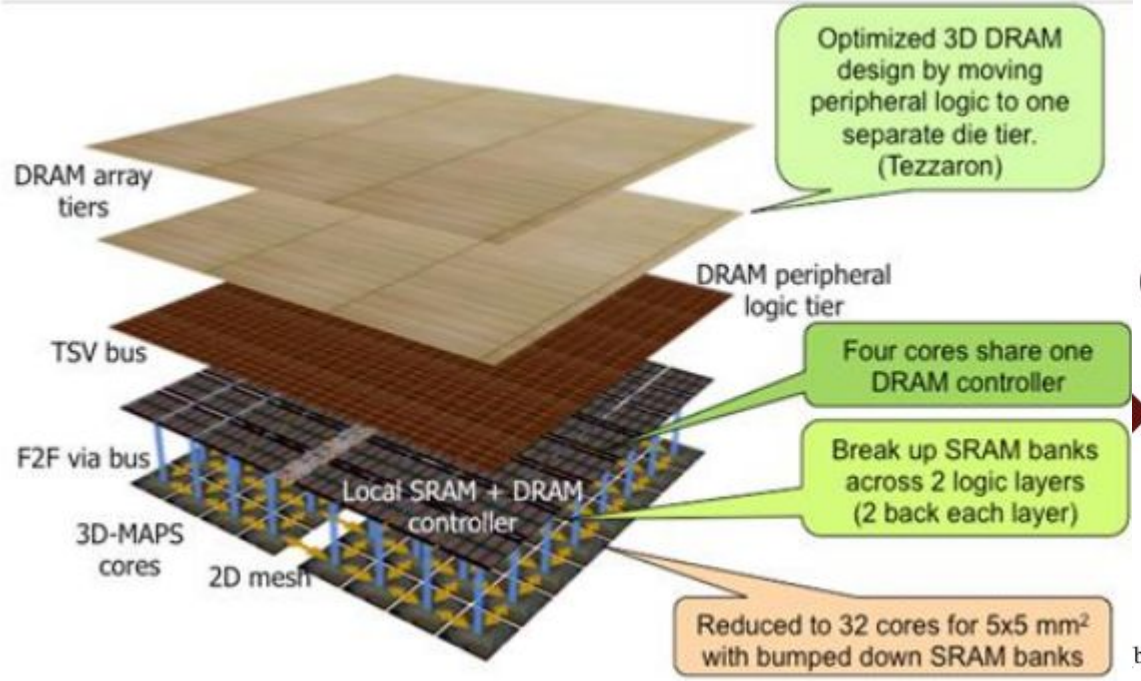


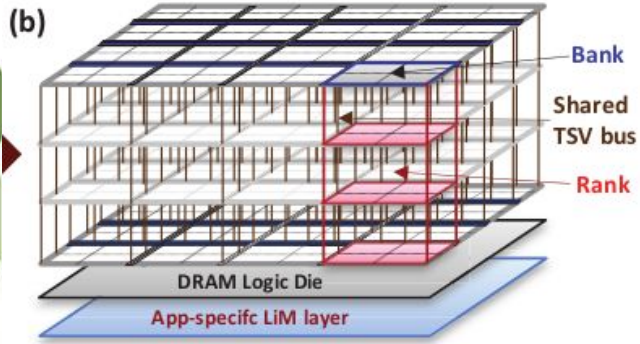
http://www.linx-consulting.com/TSV2012.html

In 2.5D

Electricity supply from Grid to building.

3D looks like this





b) Fine-grained 3D Die-stacked DRAM

Die stacking by Yuan Xie and Jishen Zhao

whatis.techtarget.com/fileformat/TSV-Tab-separated-values-file

In real it looks

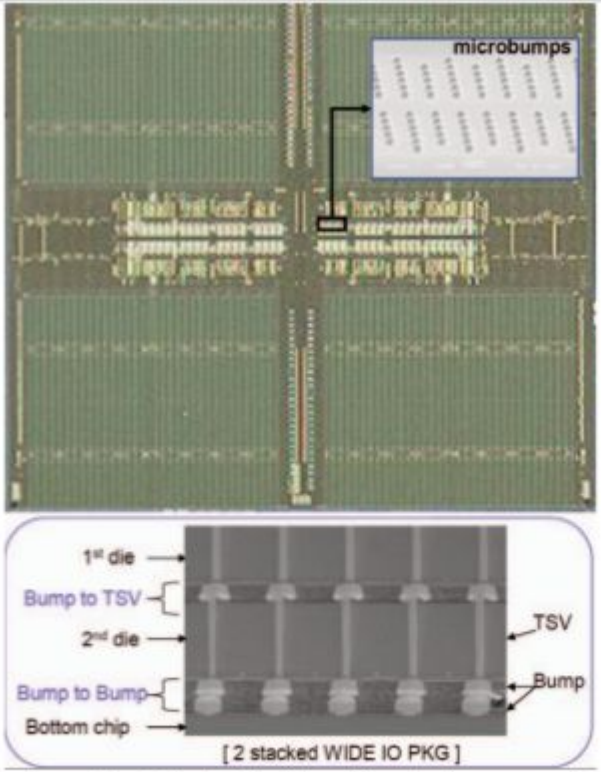


Figure 28.5.7: Photograph of fabricated chip with microbumps and vertical section of 2-stacked Wide-I/O DRAMs.

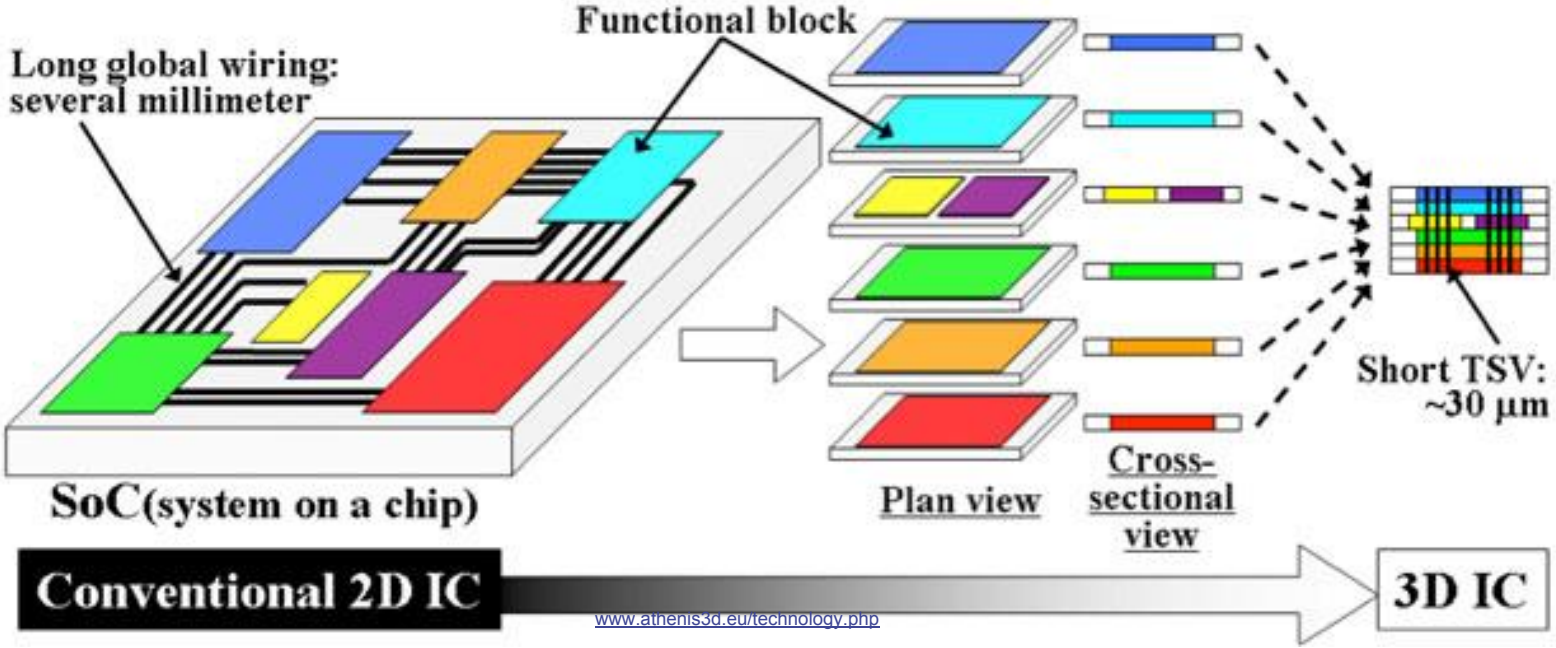
whatis.techtarget.com/fileformat/TSV-Tab-separated-values-file

©samsung wide i o

Benefits

- Low Cost
- Small Space
- Low Power
- Wide Bandwidth (in TBps)
- Shorter Interconnect/ Latency Improvement
- Heterogeneous integration

Heterogeneous integration



www.athenis3d.eu/technology.php

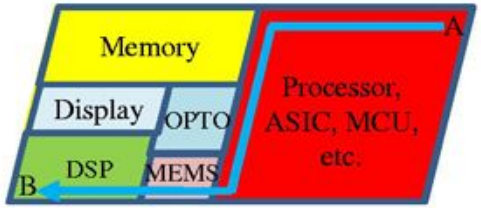
Moore's law

More than Moore

2D SoC

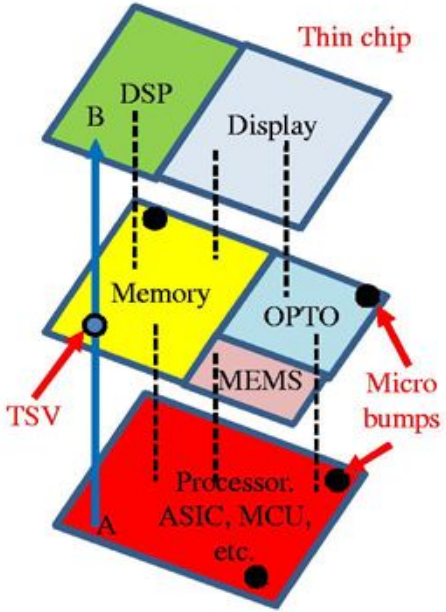
3D IC integration

3D Si integration



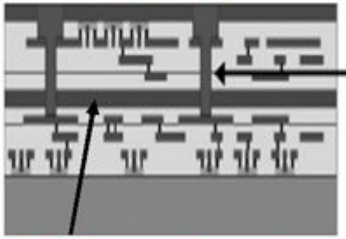
Long wiring (from A to B) in 2D SoC

For both cases, thermal management is a big issue!



Short wiring (from A to B) in 3D IC integration with TSVs, thin chips, and microbumps

Thin chips



Wafer-to-wafer bonding (bumpless)

Very short wiring in 3D Si integration with very tiny TSVs, thin wafers/chips, and bumpless (no bumps!)

Thermal management is a huge problem

http://semiconductortechnology.blogspot.in/2014/03/global-3d-ic-and-tsv-interconnect.html

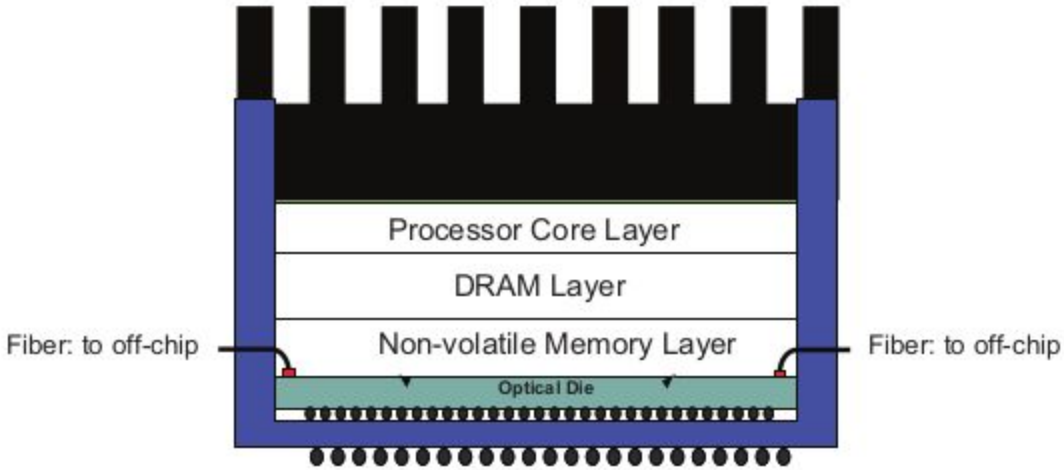


Figure 2.1: An illustration of 3D heterogeneous architecture with non-volatile memory stacking and optical die stacking.

Die stacking by Yuan Xie and Jishen Zhao

QUESTIONS

thank you!

pptbackgroun