IITK CSE RESEARCH DAY

AUGUST 9, 2025

RM101, Rajeev Motwani Building
Department of Computer Science and Engineering
Indian Institute of Technology Kanpur

Program

9:30 - 9:35	Welcome Address
9:35 - 11:00	Faculty Talks
11:00 - 11:30	Tea Break
11:30 - 13:00	Student Talks
13:00 - 14:30	Lunch
14:30 - 16:30	Poster Presentations by Students
16:30 - 17:15	Tea Break
17:15 - 18:30	*Prof. Hari Sahasrabuddhe Lecture* by **Prof. Rajeev Alur**
19:30 - 21:00	Dinner

PROF. HARI SAHASRABUDDHE LECTURE

5:15 PM – 6:30 PM

Session Chair: Prof. Indranil Saha

Learning Symbols for Trustworthy AI

– Prof. Rajeev Alur, University of Pennsylvania

Abstract: Recent advances in deep learning have led to novel AI-based solutions to challenging computational problems. Yet, the state-of-the-art models do not provide reliable explanations of how they make decisions, and can make occasional mistakes on even simple problems. The resulting lack of assurance and trust are obstacles to their adoption in safety-critical applications. Neurosymbolic learning architectures aim to address this challenge by bridging the complementary worlds of deep learning and logical reasoning via explicit symbolic representations. In this talk, I will describe representative neurosymbolic systems, and how they enable more accurate, interpretable, and domain-aware solutions to problems in healthcare and robotics.

Bio: Rajeev Alur is Zisman Family Professor of Computer and Information Science and the Founding Director of ASSET (Center for AI-Enabled Systems: Safe, Explainable, and Trustworthy) at University of Pennsylvania. He obtained his bachelor's degree in computer science from IIT Kanpur in 1987 and PhD in computer science from Stanford University in 1991. Before joining Penn in 1997, he was with Computing Science Research Center at Bell Labs. His research is focused on principles and tools for design and analysis of safe and trustworthy systems. He is a Fellow of AAAS, ACM, EATCS, and IEEE, an Alfred P. Sloan Faculty Fellow, and a Simons Investigator. Notable awards include the inaugural CAV (Computer-Aided Verification) award (2008), the inaugural Alonzo Church award (2016), IIT Kanpur Distinguished Alumnus Award (2017), the Knuth Prize (2024), and the EATCS Award (2025). He is the author of the textbook *Principles of Cyber-Physical Systems* (MIT Press, 2015), has served as the chair of ACM SIGBED (Special Interest Group on Embedded Systems), was the lead PI of the NSF Expeditions in Computing project ExCAPE on program synthesis, and is the General Chair for upcoming Federated Logic Conference (FLoC) in 2026.

FACULTY TALKS

9:35 AM – 11:00 AM

Session Chair: Prof. Sumit Ganguly

Fault-tolerant Mincuts

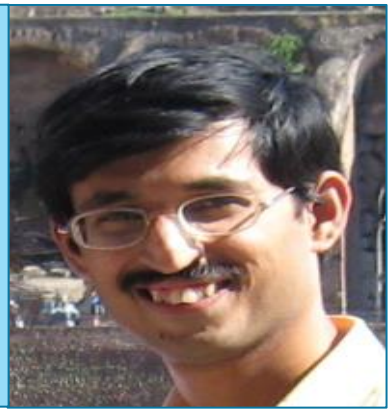
– Prof. Surender Baswana, Dept. of CSE, IIT Kanpur

Abstract: Minimum cuts (in short, mincuts) are fundamental graph structures that have been extensively researched for more than half a century. A fault-tolerant data structure for mincuts aims at answering the following query efficiently: Report a mincut between any given pair of vertices after the failure of any given edge. We shall present data structures that occupy optimal space and answer the queries very efficiently.

Bio: Surender Baswana has been a faculty member in the Department of Computer Science and Engineering at IIT Kanpur since 2006. He currently serves as the Head of the Department. His research primarily focuses on the design and analysis of efficient computer algorithms, with particular emphasis on graph algorithms, dynamic algorithms, fault-tolerant structures, and randomized algorithms. His current area of interest lies in compact structures and efficient algorithms for mincuts. His outstanding research is reflected in his extensive publications at premier conferences in theoretical computer science and algorithms, such as STOC, FOCS, and SODA. He is a recipient of the Alexander von Humboldt Fellowship for Experience Researchers (2018). He was awarded a certificate of exceptional contribution from the Director of IIT Bombay (Chairman, JAB 2015) towards the development of the software for the joint seat allocation in central government funded technical institutes of India in 2015. He is also a recipient of the Young Engineer Award from the Indian National Academy of Engineering (2009), and the Outstanding Ph.D. Dissertation Award by IBM India Research Lab (2005). In addition to his research contributions, he is widely recognized for his dedication to teaching. He has received the IIT Kanpur Distinguished Teacher Award (2017), the Gopal Das Bhandari Memorial Distinguished Teacher Award (2010), and has been honored with the Best Faculty Award by graduating batches for eight years.

Language Models for India

– Prof. Arnab Bhattacharya, Dept. of CSE, IIT Kanpur



Abstract: Language models have caught the attention of all and sundry. Unfortunately, however, large language models do not perform satisfactorily for Indian languages, Indian context, Indian culture, and Indian issues. While many of the issues are data-driven, and a lack of good corpora poses the main hindrance, there are more fundamental problems in language models pertaining to linguistics and language structure, including grammar, morphology, and vocabulary. In this talk, we will elucidate some of these issues with pointers to possible solutions.

Bio: Arnab Bhattacharya has been a faculty member in the Department of Computer Science and Engineering at IIT Kanpur since 2007. He also serves as the coordinator for ŚIKṢĀ, the Study Centre for Indian Knowledge System for Holistic Advancement. His research interests span databases, data mining, information retrieval, natural language processing, and artificial intelligence, with notable strengths in graph querying, skyline queries, and efficient indexing techniques. His outstanding research is evidenced by his extensive publications in premier computational linguistics conferences like ACL and NAACL, and data engineering conferences like ICDE, SIGMOD and VLDB. Being a prolific researcher, his works have been recognized through several prestigious honors, such as the IBM Faculty Research Award (2014) and the Yahoo! Faculty Research and Engagement Award (2011). His contributions to data mining have earned him multiple best paper awards, including the Best Paper Award at COMAD 2011 and the Best Student Paper Award for his student at COMAD 2010. Earlier, his paper was selected among the top five student papers at ICDM 2005. His contributions extend to significant sponsored projects, including "*Sanskrit Knowledge Accessor*", "*Advancement of NLP Techniques for Indian Languages with Focus on Bangla and Hindi*", and "*NYAYA: A Legal Assistance System for Legal Experts and the Common Man in India*".

Orthogonality of Core and Uncore Resource Policies in Chip-multiprocessors

– Prof. Mainak Chaudhuri, Dept. of CSE, IIT Kanpur

Abstract: Today's many-core chip-multiprocessors employ a large number of online policies to manage on-chip resources. The private caches sitting inside the cores and the shared last-level cache along with the coherence directory of the uncore are perhaps the top few resources that have first order impact on the end-to-end performance of software. The policies to manage these important resources are often not orthogonal and end up influencing each other's outcome. Non-orthogonality of these policies not only leads to performance problems, but also opens information leakage channels. In this talk, we will briefly outline how to orthogonalize the coherence directory and shared last-level cache management policies with respect to the core cache policies thereby achieving the much-needed core-uncore isolation.

Bio: Mainak Chaudhuri has been a faculty member in the Department of Computer Science and Engineering at IIT Kanpur since 2004. He served as the Head of the Department from 2020 to 2023. His primary research interest is memory system optimization for emerging many-core chip-multiprocessors. During his research career, he has made significant contributions to several areas of computer architecture, as evidenced by his extensive publications in premier conferences like ISCA, Micro, and HPCA. He was a recipient of the Best Paper Award at the Premier Computer Architecture Conference HPCA in 2005 and 2017. He was honored by Intel Corp with their 'Technology Excellence Award' as an expression of Intel India's gratitude for his exemplary contribution and commendable collaboration with Intel India. Complementing his impactful research, he is equally recognized for his excellence in teaching and was honored with the IIT Kanpur Distinguished Teacher Award (2024) and the Annual Best Teacher Award in CSE (2021 and 2023).

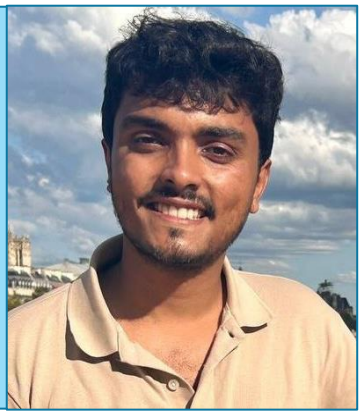
STUDENT TALKS

11:30 AM – 1:00 PM

Session Chairs: Prof. Soumya Dutta and
Prof. Sayak Ray Chowdhury

Geometry and Information

– **Akhil S**, Ph.D. Candidate, Dept. of CSE, IIT Kanpur
(Advisor: Prof. Satyadev Nandakumar)



Abstract: This talk looks at how ideas from geometry, information theory, and cryptography are connected through the concept of dimension.

Hausdorff dimension is a way to extend our usual idea of dimension, like a line being 1D or a plane being 2D, to more complicated sets. It can even describe shapes that do not have whole number dimensions, like the Sierpiński triangle.

We'll also look at a version of this idea from computer science, called constructive dimension. We see how this notion is connected to the density of information.

A key result we'll explore is the Point-to-Set Principle, which builds a bridge between Hausdorff and constructive dimension, thereby revealing deep connections between geometry and information.

Finally, we'll see a recent result from our group that links the polynomial-time version of dimension to the existence of one-way functions.

A Hardware Designer's Perspective on Lattice-based Post Quantum Cryptographic Algorithm

– **Suraj Mandal**, Ph.D. Candidate, Dept. of CSE, IIT Kanpur
(Advisor: Prof. Debapriya Basu Roy)

Abstract: Lattice-based post-quantum secure algorithms have received significant research interest due to the urgent requirement to develop a post-quantum secure framework. In the round 4 finalists announced by NIST, lattice-based algorithms like CRYSTALS-Kyber, CRYSTALS-Dilithium, and FALCON have been shortlisted, and therefore, designing an efficient architecture for these algorithms is a necessity. Executing these algorithms requires large-degree polynomial multiplication in the ring

$$R_q = Z_q [x]/X^N +1.$$

Number Theoretic Transformation (NTT) is a widely adopted methodology for computing the large degree polynomial multiplication for such lattice-based cryptographic algorithms, provided the modulus q is of the form

$$K \times 2\ m + 1 \text{ for } K \in Z.$$

The complexity of NTT multiplication is O(N log N), which is superior to other multiplication algorithms like Karatsuba or Toom-Cook. In this talk, I shall be providing a brief overview of designing efficient higher radix as well as lower radix NTT multiplication units for Lattice-based algorithms. I shall also provide an overview of the other modules, like Keccak or different samplers, used in lattice-based PQC algorithms.

Towards Understanding Commonsense and Causal Reasoning Mechanisms in Large Language Models

– **Abhinav Joshi**, Ph.D. Candidate, Dept. of CSE, IIT Kanpur
(Advisor: Prof. Ashutosh Modi)

Abstract: Understanding causal relationships is one of the core aspects of human reasoning, yet it remains a significant challenge for large language models (LLMs). In this talk, we will present **COLD** (**C**ausal reas**O**ning in c**L**osed **D**aily activities), a framework designed to understand causal reasoning in Language Models using structured, script-based descriptions of daily human activities. By constructing observational and causal graphs from crowd-sourced event sequences, COLD enables the generation of millions of causal queries grounded in real-world context and aims towards bridging the gap between real-world grounded reasoning and symbolic causal reasoning. We will also briefly touch on our related work on inspecting internal LLM mechanisms that help in making decisions during reasoning tasks. While our results provide only a partial view, we believe they contribute to a growing effort to rigorously test reasoning capabilities in LLMs.

PHALCON: Phylogeny-Aware Variant Calling from Large-Scale Single-Cell Panel Sequencing Datasets

– **Priya**, Ph.D. Candidate, Dept. of CSE, IIT Kanpur
(Advisor: Prof. Hamim Zafar)

Abstract: Single-Cell Sequencing (SCS) enables variant detection and tumor phylogeny reconstruction for resolving intra-tumor heterogeneity (ITH), which causes drug resistance and cancer relapse. Recently emerged panel sequencing methods sequence disease-specific genes across thousands of cells, but existing variant callers and SCS-specific phylogenetic methods struggle with large-scale datasets and amplification biases in panel-based sequencing protocols. We present a statistical variant caller, PHALCON for scalable mutation detection from large-scale single-cell panel sequencing data by modeling tumor evolution under a finite-sites model along a clonal phylogeny. Across a wide variety of simulated and real datasets, PHALCON outperformed state-of-the-art methods in variant calling, tumor phylogeny inference, and runtime. From triple negative breast cancer (TNBC) and acute myeloid leukemia (AML) datasets, PHALCON detected novel somatic mutations with high functional impact, resolved clonal substructure and rare clones. In AML, PHALCON also uncovered poor-survival subgroups harboring DNA methylation and chromatin/cohesin mutations and revealed novel cellular co-occurrence and exclusivity patterns of driver mutations.

N-Tracer: A Trace Driven Attack on NoC-based MPSoC

– **Dipesh**, Ph.D. Candidate, Dept. of CSE, IIT Kanpur
(Advisor: Prof. Urbi Chatterjee)

Abstract: Network-on-Chip (NoC) has emerged as a promising technology to interconnect different components of Multiprocessor System-on-Chip (MPSoC) and is preferred due to its high throughput and lower latency. Despite all its advantages, NoCs are vulnerable to side-channel attacks. Recently, researchers have demonstrated practical _time driven cache attacks_ and _access driven cache attacks_ namely Earthquake, PP-Arrow and PP-Firework on NoC to retrieve secret keys of AES. Although _trace driven cache attacks_ are more powerful due to its simplicity and enhanced key entropy reduction capabilities, no such attack has been demonstrated so far for NoC architecture. The downside could be the fact that a) the attack setup overhead is high due to the requirement of an oscilloscope, b) unavailability of hardware performance counters (HPCs) of the secure zone in the NoC. In this work we propose a novel method to monitor cache hit/miss in L1 (private) cache of AES core of the secure zone just by observing the _delay in throughput drop_ of the adversarial packets on the NoC network. This completely eliminates the above-mentioned requirements. The proposed attack is able to reduce the key search space to 2^8 with the requirement of 256 traces only.

LEOCraft: Towards Designing Performant LEO Networks

– **Suvam Basak**, Ph.D. Candidate, Dept. of CSE, IIT Kanpur
(Advisor: Prof. Amitangshu Pal)

Abstract: Low Earth Orbit (LEO) satellite constellations have revolutionized Internet access for millions of users. OneWeb and SpaceX Starlink are already operating constellations of hundreds and thousands of satellites, offering Internet service directly from space across 100+ countries. These exceptionally large networks come at a cost: thousands of routers (satellites) need to fly at ~22x the speed of sound, thus making network design a non-trivial challenge. While the systems research community with decades of deep networking expertise has a relatively short window to influence the design of these networks, there is a serious lack of the right tools to enable such efforts. To address this, we introduce LEOCraft - an LEO network design framework to help the community visualize and evaluate the performance of different choices. LEOCraft offers integrated optimization techniques tuned upon the domain knowledge acquired from thousands of LEO constellation design's performance evaluations to optimize a new constellation design ~5× faster than other off-the-shelf black-box optimization techniques. LEOCraft scales up seamlessly, tested up to 83K satellites across multiple shells (more than 2x SpaceX's long-term proposal) with 1K ground stations, thus making it feasible for the community to explore LEO trajectory and topology design for even the largest of mega-constellations.

POSTER PRESENTATIONS

2:30 PM – 4:30 PM

Session Chair: Prof. Purushottam Kar

THEORY

- **Query Complexities & Zebra Functions**
  — Premanshu Chatterjee (premanshu24@cse.iitk.ac.in)

- **One-Way Functions and Polynomial Time Dimension**
  — Suronjona Sarma (suronjona@cse.iitk.ac.in)

- **Polynomial Factorization Modulo Prime Powers**
  — Tufan Singha Mahapatra (tufansm@cse.iitk.ac.in)

ARTIFICIAL INTELLIGENCE / MACHINE LEARNING

- **Linguistic Inspired Pose-Stitching for End-to-End Sign Language Translation**
  — Sanjeet Singh (sanjeet@cse.iitk.ac.in)

- **Uncertainty-informed Volume Visualization using Implicit Neural Representation**
  — Shanu Saklani (saklanishanu@gmail.com)

- **Towards Quantifying Commonsense Reasoning with Mechanistic Insights**
  — Abhinav Joshi (ajoshi@cse.iitk.ac.in)

- **PHALCON: Phylogeny-Aware Variant Calling from Large-Scale Single-Cell Panel Sequencing Datasets**
  — Priya (priya22@iitk.ac.in)

- **Towards Robust Evaluation of Unlearning in LLMs via Data Transformations**
  — Divyaksh Shukla (divyaksh@cse.iitk.ac.in)

- **A Scalable Multi-Robot Goal Assignment Algorithm for Minimizing Mission Time followed by Total Movement Cost**
  — Aakash (aakashp@cse.iitk.ac.in)

ARTIFICIAL INTELLIGENCE / MACHINE LEARNING

- **Leveraging LLMs for Bangla Grammar Error Correction: Error Categorization, Synthetic Data, and Model Evaluation**
  - Pramit Bhattacharyya (pramitb@cse.iitk.ac.in)

- **Graph-Based Resource Allocation in Wireless Networks Using Policy Gradient RL**
  - Abhinav Anand (abhinavanand@cse.iitk.ac.in)

- **Understanding memorization in DNNs**
  - Aishwarya Gupta (aishwaryag@cse.iitk.ac.in)

SYSTEMS

- **Scalable Prediction and Visualization of Extreme Weather Events**
  — Muzafar Ahmad Wani (muzafarwan@cse.iitk.ac.in)

- **Pre-emptive Memory Protection Promotion for Unified Memory GPU Programming**
  — Pranjal Singh (prsingh@cse.iitk.ac.in)

- **AH-TLB: Efficient Address Translation in GPUs using Anticipatory Huge TLB Entries**
  — Binong Kiri Bey (binong@cse.iitk.ac.in)

- **Measuring Orbital Shifts Due to Solar Radiation**
  — Suvam Basak (suvambasak@cse.iitk.ac.in)

- **SCRUBD: Smart Contracts Reentrancy and Unhandled Exceptions Dataset**
  — Chavhan Sujeet Yashavant (sujeetc@cse.iitk.ac.in)

- **LRHAR: A Lightweight Rule-based Framework for Human Activity Recognition at the Edge**
  — Shaijal Tripath (tripjal@cse.iitk.ac.in)

SYSTEMS

- **LeakyRand: An Efficient High-fidelity Covert Channel in Fully Associative Last-level Caches with Random Eviction**
  — Yashika Verma (yashikav@cse.iitk.ac.in)

- **Through-the-Wall Multi-Person Localization using Translation and Rotation Synthetic Aperture Radar**
  — Ashutosh Deshwal (ashutosh@cse.iitk.ac.in)

- **Phase-based Performance Analysis and Modeling of HPC Applications**
  — Vishal Deka (vdeka@cse.iitk.ac.in)

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